

THE UNIVERSITY OF CHICAGO

CHEMICAL TUNING OF THE ELECTRONIC PROPERTIES OF ATOMICALLY THIN
SEMICONDUCTORS

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PREETI KUMARI PODDAR

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To my family

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ABSTRACT

Monolayers of transition metal dichalcogenides (TMDs) provide high performance semiconductor films for developing atomically thin devices and circuitry. Realizing this on a large, technologically relevant scale requires the ability to control their electronic properties (*e.g.*, *p*-type vs *n*-type) precisely for reproducible device performance with minimum device-to-device variation. Currently, one of the major sources of hindrance towards achieving this is the use of conventional resist-based lithography for their device fabrication. Photolithography and electron-beam lithography are the most common methods for making nanoscale devices from semiconductors. However, their influence can be more crucial for atomically thin semiconductors compared to bulk semiconductors due to the atomic thinness and all-surface nature of the former. Monolayer TMDs are extremely sensitive to the surface exposure to chemicals (solvents, resists, hot metals, etc.) involved in conventional lithography processes. The unintentional changes to the TMDs make it difficult to fabricate devices with predictable performance. In this thesis, we will address this challenge. First, we will introduce a resist-free non-perturbative approach for fabrication of TMD-based devices and their electrical measurement with minimum change to their pristine properties. We will use this method to characterize the electrical conductivity of as-grown monolayers of TMDs and then study the unintentional doping caused during various stages of conventional lithography-based fabrication process. Second, using this method we will precisely study the tuning of electrical conductivity of TMDs which is achieved through substitutional doping. Our study explains the difference in the dopant behaviors in two-dimensional semiconductors compared to their 3D counterparts. The methodology that is discussed here will enable the development of a rational and reproducible process design for large-scale integrated circuits based on TMDs and other surface-sensitive materials.

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CHAPTER 1

INTRODUCTION AND OVERVIEW

1.1 Introduction

The foundation of this dissertation is formed by the two-dimensional (2D) materials, specifically transition metal dichalcogenides (TMDs) and their electronic properties. The surge of interest in 2D materials that started from the isolation of graphene in 2004 has given way to generation and exploration of numerous other such materials.¹⁻³ TMDs are the most extensively researched 2D materials after graphene due to their remarkable mechanical, optical and electronic properties.⁴⁻⁸ From electronics point of view, 2D materials exhibit a wide range of properties and can be metallic, semiconducting or superconducting.³ Here we will mainly focus on single layer of semiconducting TMDs *e.g.*, MoS₂, WSe₂ which are only three atoms thick.

With the continuous need of thinner channels for future electronics, monolayer TMDs provide an ideal platform to realize integrated circuitry in atomic thickness limit. Semiconductor monolayer TMDs have finite band gaps (1–2 eV) and therefore, for electronic devices such as field-effect transistors (FETs) that require to turn on and off the channels, they have indeed shown large switching ratios as well as high carrier mobilities.⁹⁻¹³ However, one thing to note when considering a transition from conventional bulk semiconductors to atomically-thin semiconductors is that the properties of the materials change drastically in this regime, be it optical, mechanical or electrical. One stark difference is that two-dimensional materials have much larger surface to volume ratios and the electric current flows through their surfaces unlike in bulk semiconductors.

The all-surface nature of monolayer TMDs with electrons propagating through their surfaces is one of their important features with additional consequences. In the monolayer limit, there is reduced dielectric screening of Coulomb interaction between charge carriers on either side

of the semiconductor surface which makes their electronic properties extremely sensitive to environmental variations. These variations can be broadly of two types: 1) ones that are intentional and controlled, *e.g.*, electrostatic gating to modulate the polarity of charge carriers and their densities or deposition of a high dielectric constant oxide, and 2) ones that are unintentional and can arise due to reasons such as during device fabrication processes and applied chemicals. The initial motivation of this thesis is to identify and isolate second type of variations *i.e.*, the factors during device fabrication of monolayer TMD-based devices, the contributions of which are uncontrolled and that can unintentionally alter semiconductor electronic properties and the final device performance. The currently used approaches for device fabrication are borrowed from bulk semiconductors¹⁴ and are predominantly electron beam lithography and photolithography.^{9-13,17,18} Hence, many steps in conventional lithography processes that are performed on the surface of materials (*e.g.*, resist coating, exposure to ultraviolet light, solvent for development and cleaning) may modify their electrical properties, as illustrated in Fig. 1.

The perturbations to the monolayer TMDs during device fabrication can pose important technical challenge in realizing devices and circuitry based on them. It is known that the performance of semiconductor devices in integrated circuits is determined by the properties of the semiconductor material (*e.g.*, *p*-type vs *n*-type) as well as the effects of subsequent processes that are carried out on the material during device fabrication.¹⁴ The contribution from the latter as discussed above becomes more significant in atomically thin materials. Another technical challenge is that TMDs are atomically thin and thus, easy to damage. For example, direct evaporation of hot metals for electrical contacts is known to affect the overall electrical device conductivity.^{15,16} For this reason, different electrical properties can be seen even when the same starting material is used to fabricate devices using procedures involving different chemicals and

processes. The challenge, therefore, is to carefully control the electrical properties of the starting material, often as-grown thin films, and understand the effects of individual device fabrication step on the material. This is necessary for reliable and desired device performances based on monolayer TMDs. While both these capabilities are ubiquitous in bulk semiconductor processing, they are not available for monolayer TMDs.

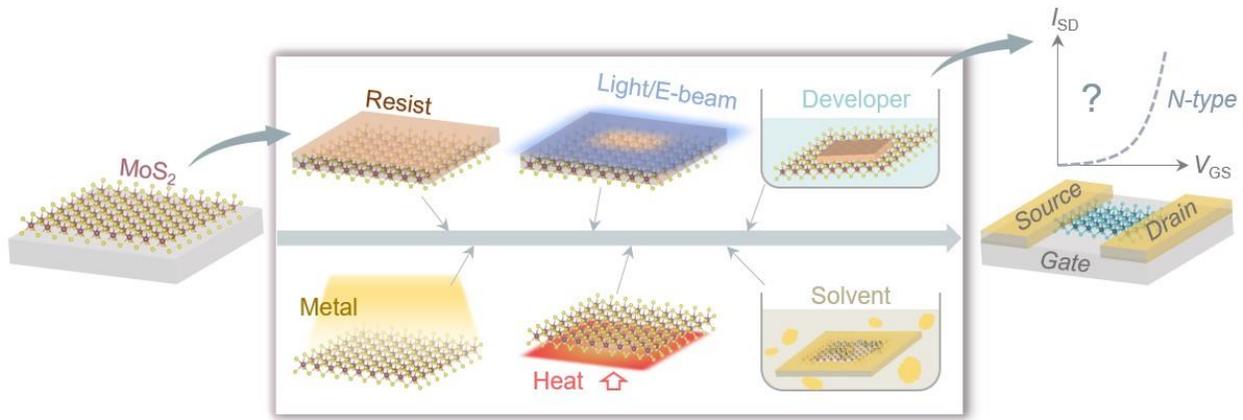


Figure 1.1 Contributions from device fabrication to electrical properties of monolayer TMDs during lithography-based device fabrication. Schematic showing various steps of conventional lithography process, which when carried out on as-grown monolayer TMD, here, MoS₂ may affect the final measured device properties (the predominant *n*-type semiconductor behavior). Examples include resist coating, UV light or e-beam exposure, development, metal deposition, heating and resist removal or cleaning in solvents.

1.2 Outline of the dissertation

In this dissertation, we will present our approach to address the above challenges. The thesis is organized as following. We will first review in Chapter 2, the structure of monolayer TMDs that give rise to their distinct electronic properties followed by discussion of their prominent optoelectronic properties. Towards the end of the chapter, we will touch upon their large-scale synthesis which brings them closer to technological applications.

In Chapter 3, we will review the main factors that can affect the electronic properties of monolayer TMDs. It is important to understand the various contributions that lead to the measured electrical properties of TMD based devices.

We will start Chapter 4 with a discussion about existing lithography-based electrical measurement/device fabrication approaches commonly used for atomically thin semiconductors. We will discuss their limitations and briefly review previous works that have been done to address them. Following this, we will introduce our non-perturbative electrical measurement approach ideal for atomically thin semiconductors with minimum changes to their properties. This method will serve as a tool for precise chemical tuning of the electronic properties of TMDs.

In Chapter 5, we will discuss the electrical properties of as grown monolayers of MoS₂ and WSe₂ that are measured non-perturbatively. We will compare them with those of channels measured using lithography-based measurement to distinguish the net effects of processing during lithography-based device fabrication. Furthermore, we will use the non-perturbative method to systematically monitor the electrical properties of channels at various stages of common lithography-based fabrication processes. One surprising observation is that simple exposures to solvents like acetone can change the electrical conductivity of MoS₂ much more than the rest of the processes. We will further show that such change can be interpreted as a doping effect, the degree of which can vary for solvents with different electronegativities. Therefore, solvent-induced doping can serve as a knob for chemical tuning of electrical properties of TMDs.

In Chapter 6, we will extend the utility of the non-perturbative measurement. We study the precise chemical tuning of electrical conductivity of semiconducting TMDs through substitutional doping, which is achieved via a controllable synthesis technique. Finally, in Chapter 7, we will touch upon several future directions.

CHAPTER 2

ATOMICALLY THIN TRANSITION METAL DICHALCOGENIDES

2.1 Introduction

In this Chapter, we will review the basic crystal structures, electrical and optical properties of monolayer semiconducting TMDs. We discuss their optical properties useful for the characterization of TMDs and electrical properties important for understanding the field effect transistor devices. At the end, we will discuss growth methods for their large-scale synthesis.

2.2 Crystal Structure and Origin of Electronic Properties

Transition metal dichalcogenides are a group of materials with the general chemical formula MX_2 , where M is a transition metal atom of groups 4-10 (*e.g.*, Mo, W, Ti, Nb, Zr, Ta) and X is a chalcogen atom (*e.g.*, S, Se, Te). Layered or non-layered bulk materials can be thinned down to the atomic thickness to produce 2D materials. An advantage of layered structures is that the different layers interact with each other by weak van der Waals (vdW) forces while the M-X bonds in each layer are covalent in nature. This enables facile isolation of one to few layers by mechanical cleavage. A TMD monolayer is typically 6-7 Å thick and consists of a hexagonally packed layer of metal atoms sandwiched between two layers of chalcogen atoms (Figure 2.1a). The metal atom coordinates with chalcogen atoms in two different coordination geometries, namely trigonal prismatic (Figure 2.1b) and octahedral (Figure 2.1c). The variations in coordination geometry results in polymorphism in bulk forms of TMDs as an individual layer can have two prominent crystal phases: 2H (trigonal prismatic metal coordination) and 1T (octahedral metal coordination).¹⁹

The different stacking arrangements of chalcogen and metal atoms significantly affect the electronic properties of monolayer TMDs. For example, 2H-MoS₂ which is the stable phase, is

semiconducting in nature while the metastable 1T phase of MoS₂ is metallic. Phase transformation can be induced in monolayer TMDs simply by distorting their crystal lattices and is therefore, an effective way to tune their electronic properties.¹⁹⁻²³

Different electronic properties in TMDs can be explained using the ligand field theory. The coordination environment of the metal (M⁺⁴) and its *d*-electron count influence the electronic

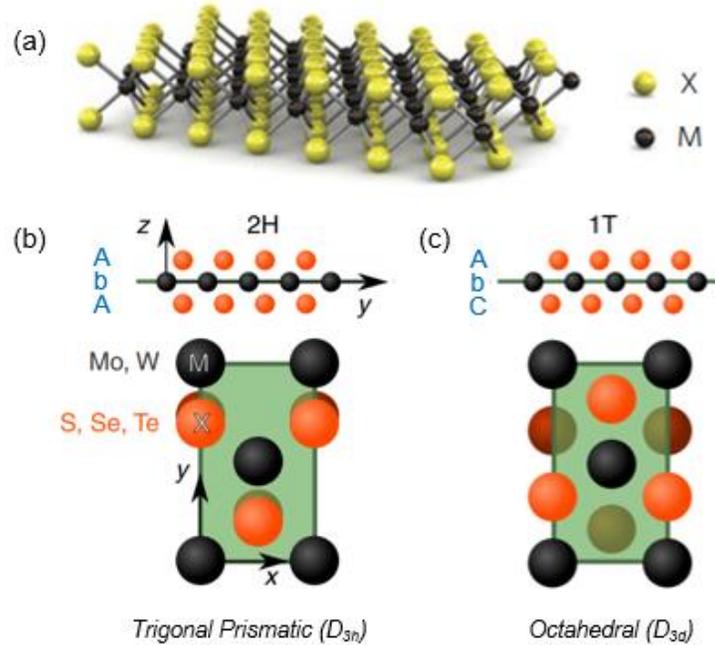


Figure 2.1 Structure and crystal phases in TMDs. (a) Schematic of monolayer TMD, MX₂. (b) Schematic of trigonal prismatic (2H phase) metal coordination with A-b-A stacking sequence of X-M-X layers. (c) Schematic of octahedral (1T phase) metal coordination with A-b-C stacking sequence of X-M-X layers. (a) Reproduced from Ref. 6 and (b), (c) from Ref. 23.

structures and location of Fermi levels in monolayer TMDs as explained in Ref. 19. Briefly, depending on the metal coordinations, there is a difference in the way *d*-orbitals split into non-bonding *d*-bands that are located within their band gaps between the bonding states (σ) and antibonding states (σ^*) of M-X bonds (Figure 2.2). This influences how electrons fill the non-bonding *d*-bands and where the Fermi level lies. For example, the resultant t_{2g} and e_g orbitals for octahedral coordination in the case of 1T-ReS₂ (d^3) will half-fill the bottom t_{2g} orbitals such that

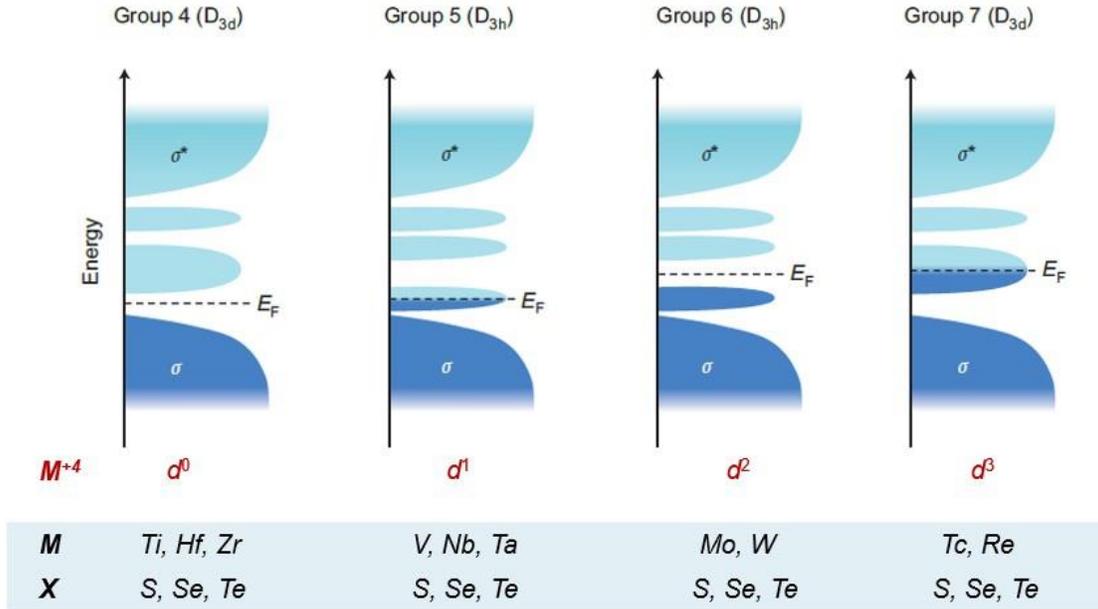


Figure 2.2 Electronic structure of various TMDs illustrated using orbital picture. Schematic showing filling of d orbitals within bonding (σ) and antibonding (σ^*) states in group 4 to 7 TMDs. The model assumes ideal coordination. The filled and unfilled states are shaded with dark and light blue, respectively. According to ligand field theory, D_{3d} compounds form two non-bonding d orbitals, $d_{yz,xz,xy}$ (t_{2g}) (bottom) and d_{z^2,x^2-y^2} (e_g) (top), while D_{3h} compounds form three d orbitals: d_z^2 (a_1), $d_{x^2-y^2,xy}$ (e) and $d_{xz,yz}$ (e') (from bottom to top). When an orbital is partially filled (e.g., group 5 and 7 TMDs), the Fermi level (E_F) is within the band and the compound exhibits a metallic character. When an orbital is fully filled (e.g., group 6 TMDs), the E_F is in the energy gap and a semiconducting character is observed. M and X denote transition metal atoms in different groups and chalcogen atoms respectively. Reproduced from Ref. 19.

the fermi level is within the band and the compound is metallic. On the other hand, the result a_1 , e and e' groups of orbitals for trigonal prismatic coordination in the case of say, 2H-MoS₂ (d^2) will fully fill the bottom a_1 orbitals such that the fermi level is in the energy gap leading to it being semiconducting. We will particularly focus on 2H-phase semiconducting Group 6 TMDs (primarily MoS₂, WS₂, MoSe₂ and WSe₂) for the rest of the thesis which will be referred to as simply TMDs unless stated otherwise.

2.3 Electrical and Optical Properties of 2D Semiconductor TMDs

Basic band structure and band offsets

One of the distinctive electronic properties of TMDs arises when the number of layers is reduced down to monolayer limit. It was first reported in 2010.^{24,25} Bulk MoS₂ is a semiconductor with an indirect bandgap of 1.3 eV, but due to quantum confinement, the bandgap of MoS₂ increases with decreasing thickness. In the monolayer limit, it becomes a direct bandgap (~1.9 eV) semiconductor. The direct band gap of monolayer MoS₂ results in a sharp absorption edge at the bandgap energy (A exciton peak). When compared to that of bilayer (Figure 2.3b), a significantly higher photoluminescence quantum yield (more than 100 times) is observed for the monolayers for the A exciton peak. Strong photoluminescence has become one of the most common ways to characterize the monolayer TMDs.

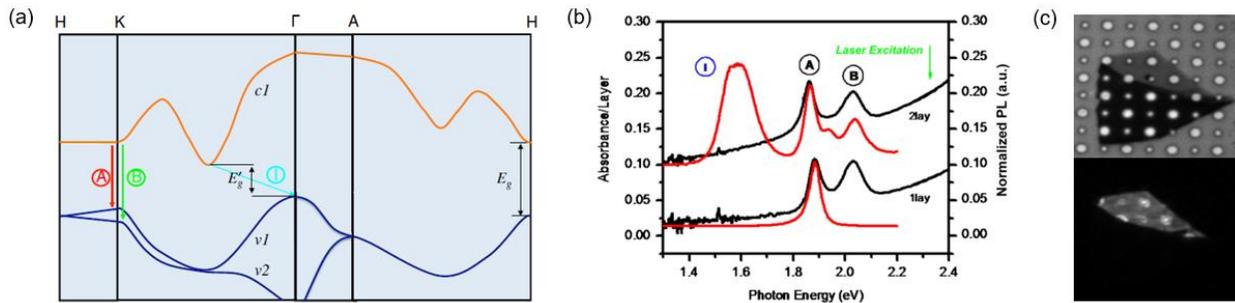


Figure 2.3 Indirect to direct bandgap transition in MoS₂. (a) Simplified band structure of bulk MoS₂, showing the lowest conduction band *c1* and the highest split valence bands *v1* and *v2*. A and B are the direct-gap transitions, and I is the indirect-gap transition. E_g' is the indirect gap for the bulk, and E_g is the direct gap for the monolayer. (b) Optical absorption (black) and photoluminescence (red) spectra of two-layer and monolayer MoS₂. A and B denotes the excitonic peaks and I is the indirect gap peak. (c) (top) optical image and (bottom) photoluminescence image of an exfoliated MoS₂ flake containing both monolayer and two-layer regions. Reproduced from Ref. 24.

The semiconductor TMDs exhibit different band offsets, the trends of which stem from the physical origin of the conduction band minimum (CBM) and valence band maximum (VBM) located at the *K* symmetry points as well as strong spin-orbit splitting in the valence band.²⁶ An

advantage of the variable band gaps of TMDs extending from visible to near-infrared photon energies is that they can be used for multiple applications. For example, wide band gap MoS₂ or WSe₂ can be used for digital logic transistors that require a high on/off ratio, while MoTe₂ with a narrower band gap can be used for infrared detectors or light emitting diodes.²⁷ Moreover, the availability of TMDs with different band alignments allows for band gap engineering of heterostructures, offering a promising way to design functional heterostructures such as *p-n* junction diodes.²⁸ A summary of band gaps and band offsets is shown in Figure 2.4.

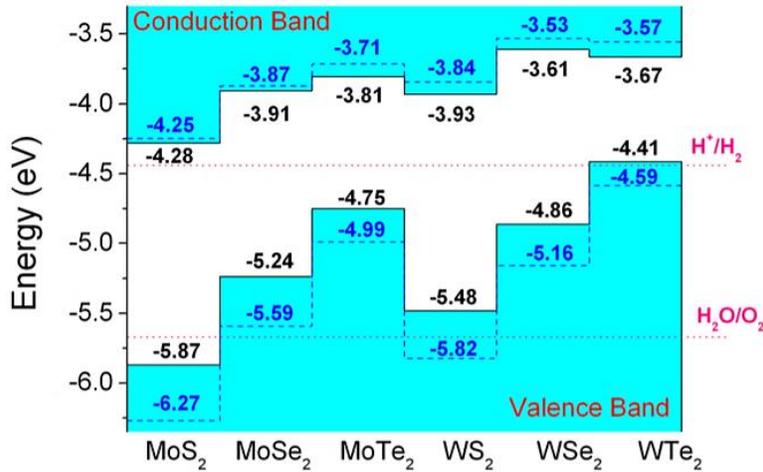


Figure 2.4 Band offsets and band gaps in monolayer TMDs. Calculated band alignment for TMD monolayers. Solid lines are obtained by Perdew-Burke-Ernzerhof exchange-correlation functional, and dashed lines are obtained by Heyd-Scuseria-Ernzerhof hybrid functional. The dotted lines indicate the water reduction (H^+/H_2) and oxidation (H_2O/O_2) potentials. Reproduced from Ref. 26.

Coulomb bound electron-hole pairs: Optical and Free-particle band gaps

Monolayer TMDs have sharp A and B absorption peaks. Such absorption peaks originate due to the presence of strong excitonic effects in these materials. Due to these effects, the band gaps in monolayer TMDs have two different values: optical and free-particle bandgap. Basically, the difference arises based on the way TMDs are excited and how the generated quasiparticles

interact. Electronic excitations are collective phenomena and are described by a quasiparticle band structure that condenses the excitations into particles with momentum and energy. In other words, the energy that is required to create an unbound electron-hole pair in the continuum is referred to as the “*free-particle or quasiparticle*” band gap. This governs the electronic properties in TMDs such as transport, contacts and band alignment in heterostructures. On the other hand, when TMDs are photoexcited, an exciton bound by attractive Coulomb forces is generated. The binding energies of excitons are large for monolayer TMDs (0.5–1 eV, corresponding to an exciton Bohr radius of ~ 1 nm)⁴. The Coulomb interactions result in excitonic resonances below the free-particle band gap. The *optical* band gap is then defined with respect to the lowest-energy excitonic feature in absorption spectra *i.e.*, the ground state of the exciton ($n = 1$) (Figure 2.5). The *free-particle* band gap corresponds to the $n = \infty$ limit of the bound exciton state and is larger than the *optical* band gap. The *free-particle* band gaps of monolayer TMDs will be used later in chapter 5 to understand their pristine electron transport properties.

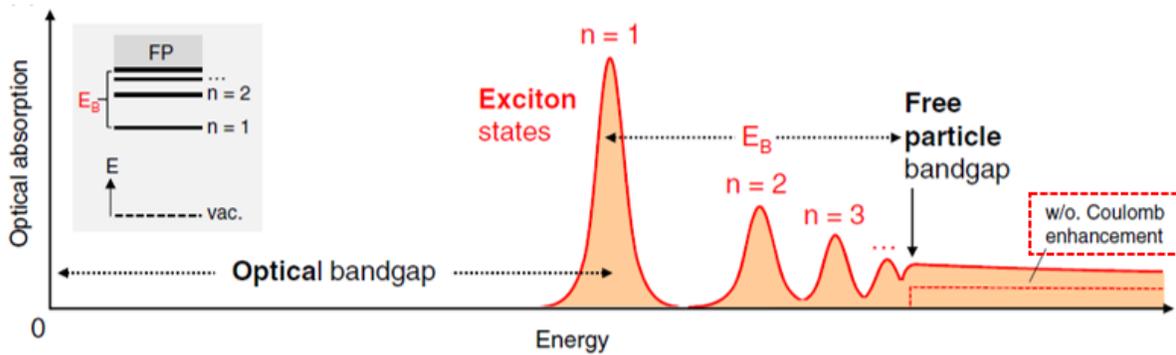


Figure 2.5 Excitonic effect in 2D semiconductor. Illustration of optical absorption of an ideal 2D semiconductor including the sharp resonance features below the renormalized quasiparticle band gap. Coulomb interaction leads to enhancement of continuum absorption for energies exceeding exciton binding energy, E_B . The absorption without Coulomb interaction exhibits a step like function. The inset shows the atom-like energy level scheme of the exciton states, designated by their principal quantum number n , with the binding energy of the exciton ground state ($n = 1$) denoted by E_B below the free-particle (FP) band gap. Reproduced from Ref. 29.

Electric field effect in TMDs

The ability to control the electronic properties of a material by an externally applied voltage forms the basis of modern electronics. For a given semiconductor material at a constant temperature, the carrier concentration is constant. One of the ways to vary the carrier concentration in a semiconductor device and thereby, change the electric conductivity at a given temperature is by applying an electric field. One device that uses this is a field-effect transistor (FET).³⁰ A typical FET includes three terminals (source, drain and gate) and a semiconducting channel. In a monolayer TMD based FET (Figure 2.6), the TMD monolayer forms the active channel between the source and drain electrodes. The electric current is injected into the channel from the source and collected at the drain by applying a bias voltage (V_{SD}). By applying a voltage to the third gate electrode (V_{BG}) that is separated from the channel by a layer of dielectric, an electric field is generated between the gate and the channel which modulates the flow of current (I_{SD}) in the channel.⁹ More specifically, for a n -type (p -type) semiconductor which has the fermi level close to its conduction band (valence band) edge, applying a negative (positive) voltage to the semiconductor or positive (negative) V_{BG} can increase the electron (hole) carrier density and produce a larger current.

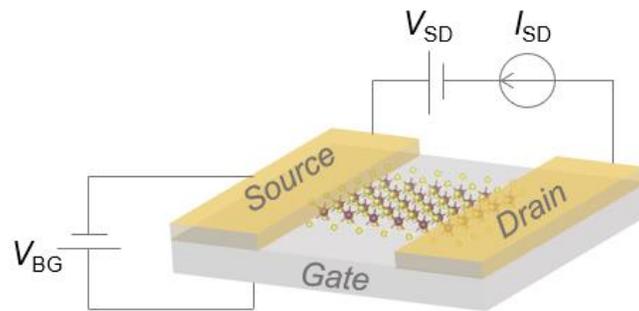


Figure 2.6 Schematic of a monolayer MoS₂ FET. Schematic of a FET with MoS₂ as the active channel and source, drain, gate terminals. V_{SD} , I_{SD} are source drain bias and current respectively, and V_{BG} is the back gate voltage.

The two important parameters that characterize the performance of FET devices are field-effect mobility and current on-off ratio. The field-effect mobility can be measured from $\mu_{\text{FE}} = \frac{1}{C_g} \times \frac{d\sigma_{\square}}{dV_{\text{BG}}}$, where C_g is the capacitance of the gate dielectric per unit area and σ_{\square} is the sheet conductivity of the channel, given by $\sigma_{\square} = \frac{I_{SD}}{V_{SD}} \times \frac{L}{W}$ with L and W being the length and width of the channel respectively. We will be extensively using this FET geometry with a back gate throughout our discussions. The transport of electrons or current in atomically thin semiconductors is only through the surface of the semiconductor, given its all-surface nature, thereby making their transport properties sensitive to their surroundings. This is different from the case of bulk semiconductors.

TMDs as channels in FETs

TMDs have a few advantages over the conventional bulk semiconductors like silicon as illustrated in Figure 2.7. The main advantage of TMDs as channels comes from their smooth surfaces without any unsaturated bonds. Presence of dangling bonds could otherwise act as charge trap centers for electrons or holes and can lead to charge scattering. For this reason, mobility degrades sharply when bulk semiconductors are thinned down to atomic thickness limit, a regime where 2D crystals facilitate much better charge transport.³¹ Also, when considering scaling down the channel lengths, the two important requirements are efficient gate control over the channel and minimum source to drain tunneling current in the off state of transistor. Monolayer TMDs have reduced dielectric screening of Coulomb interaction between charge carriers which enables excellent gate electrostatic control of the channel. Moreover, they have higher effective carrier

mass along the direction of charge transport which suppresses the source to drain tunneling probability.³¹⁻³³

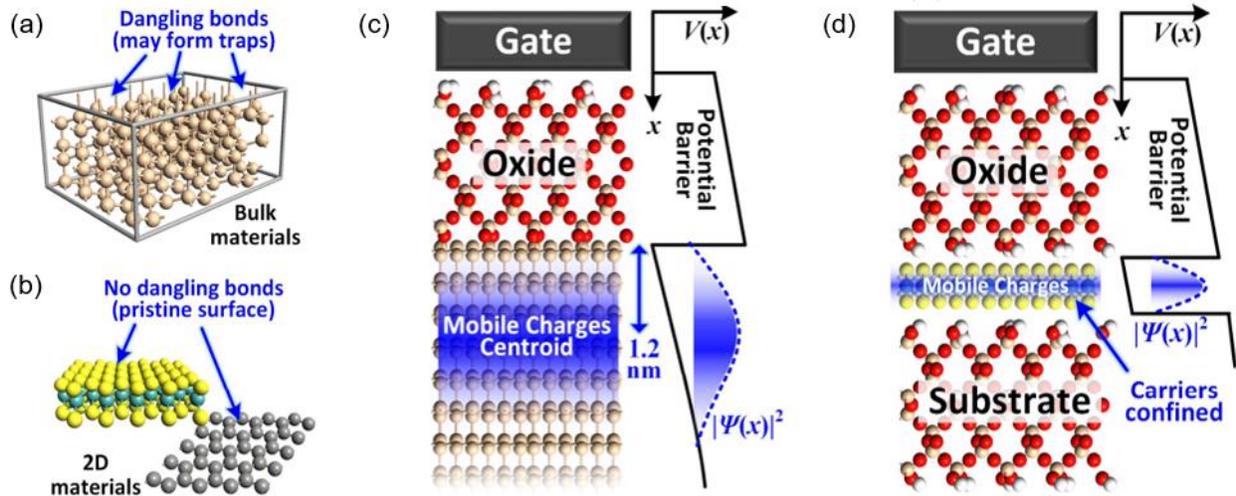


Figure 2.7 Advantages of monolayer TMDs over bulk semiconductors for electronic devices. (a) Surface dangling bonds in 3D semiconductors that can trap charge carriers and degrade device performance. (b) In contrast, 2D semiconductors have saturated bonds on their surfaces. (c) Mobile charge distribution when 3D crystals are used as channels. $V(x)$ is the gate electrostatic potential as a function of distance x . The carrier distribution given by probability function, $|\Psi(x)|^2$ extends much further from the channel dielectric interface. (d) In contrast, for 2D crystals as channels, the carriers are confined within the atomic thickness and the carrier distribution is narrower ensuring better gate control and reduced source to drain current leakage. Reproduced from Ref. 31.

Due to above mentioned features, TMD based FETs have indeed shown high device performances. Monolayer MoS₂ FETs exhibit a typical *n*-type semiconductor behavior (Figure 2.8a) and mobilities as high as ~ 60 cm²/V·s at room temperature and ~ 1000 cm²/V·s at low temperature.^{11,13} A high current on/off ratio, $\sim 10^8$ has also been achieved.¹³ Moreover, due to the improved device electrostatics, MoS₂ transistors with 1 nm gate length has displayed lower source to drain tunneling leakage compared to silicon FETs.¹² Monolayer WSe₂ FETs typically exhibit *p*-type transistor behavior (Figure 2.8b). They also show a high mobility of ~ 250 cm²/V·s and good

switching characteristics.¹⁰ Despite their atomic thinness, TMDs are undoubtedly one of the most promising candidates for future optoelectronic applications.

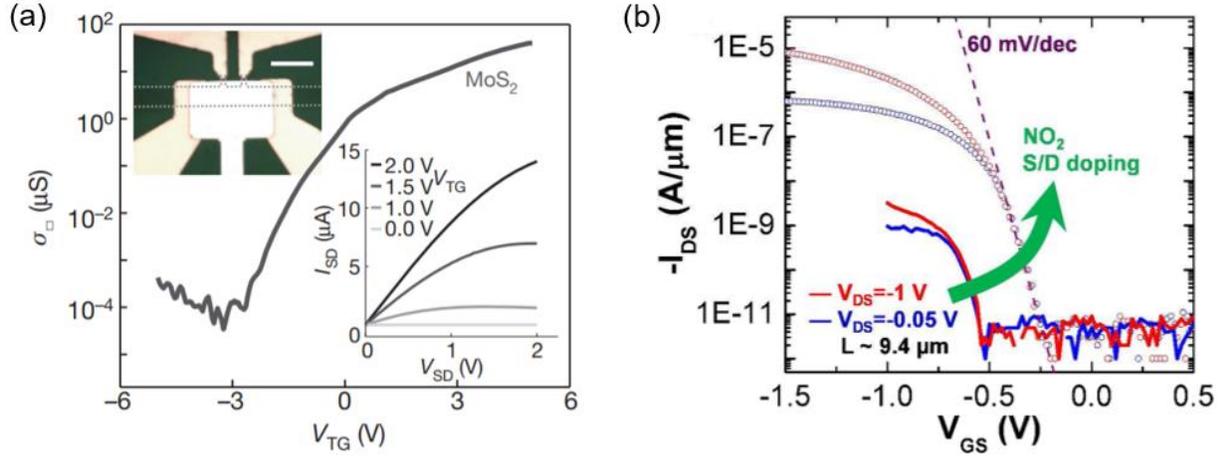


Figure 2.8 Transport in monolayer MoS₂ and WSe₂ FETs. (a) Top gate dependent *n*-type conductivity for dual-gate monolayer MoS₂ FET (device shown in the upper inset). Lower inset: Back gate voltage-dependent I_{SD} – V_{SD} curves showing current saturation and ohmic electrode contact. Scale bar, 10 μm . (b) Current vs back gate voltage transfer curves for monolayer WSe₂ devices that show a *p*-type transistor behavior. (a) and (b) have been reproduced from Ref. 18 and Ref. 10 respectively.

2.4 Large-Scale Synthesis of Monolayer TMDs

In order to fully utilize the potential TMDs hold and advance their material research to real world applications, it is necessary to produce them over large-scale with uniform thickness and properties. The mechanical exfoliation of crystals from their bulk forms is an easy and popular method to generate mono- to few layers 2D materials.^{1,9,35,36} However, the materials produced in this way are only micrometer sized flakes. This limits their scope to mostly fundamental studies and proof-of-concept demonstrations. Synthesis of monolayer TMDs, on the other hand, is a bottom-up strategy which aims at producing films through growth. Various synthetic routes such as thermolysis of ammonium thiomolybdates,^{37,38} sulfurization (or selenization) of metal (or metal oxide) thin films,^{39,40} physical vapor transport,^{41,42} and chemical vapor deposition⁴³⁻⁴⁵ have been

developed. Among these methods, vapor phase deposition has shown great promise towards high-quality TMD growth over larger scales.

Chemical vapor deposition (CVD) synthesis relies on vaporization of solid-state metal and chalcogen precursors following which the precursors react to form the TMD. The partial pressures of the gaseous species are controlled by modulating the temperature of chalcogen and metal precursors which governs subsequent adsorption and surface reaction on the substrates. However, because the vapor pressures of solid phase precursors can vary over time, it is difficult to control their flow precisely during the entire growth time. This leads to inhomogeneous nucleation of TMD crystals that results in growth of discontinuous flakes.^{43,44} The inability to produce continuous monolayer films over large-scale limits its utility for practical purposes.

Metal-Organic Chemical Vapor Deposition for Monolayer TMDs

The metal-organic chemical vapor deposition (MOCVD) method for wafer-scale growth of monolayer TMDs (MoS_2 , WS_2) was demonstrated by several research groups including our group in 2015.²⁴ The one crucial feature that distinguishes this approach from powder CVD synthesis discussed above is the use of highly volatile gas phase precursors for both metal and chalcogen atoms, where the concentration of each reactant is precisely and separately controlled, allowing for their uniform flow during the growth. The schematic of the growth setup is shown in Figure 2.9a. The growth is carried out in a hot-wall quartz tube furnace. For example, molybdenum hexacarbonyl ($\text{Mo}(\text{CO})_6$), tungsten hexacarbonyl ($\text{W}(\text{CO})_6$) and diethyl sulfide ($(\text{C}_2\text{H}_5)_2\text{S}$), which have high equilibrium vapour pressures near room temperature are selected as chemical precursors for Mo, W, S, respectively. All of them are introduced into the furnace in gas phase. Carrier gases H_2 and Ar are injected into the chamber using separate lines. The concentration of each reactant is precisely controlled throughout the growth time by regulating their partial pressures with mass

flow controllers (MFCs). With careful optimization of growth parameters, monolayers of MoS₂ and WS₂ are grown on a 4-inch wafer scale as shown in Figure 2.9b. The films are grown in the layer-by-layer growth mode, which is ideal for the uniform layer control over large scale. Figure 2.9c shows optical images of MoS₂ films, at different growth times (t), revealing the initial nucleation on the SiO₂ surface ($t = t_0$), subsequent monolayer growth near ($0.8 t_0$) and at the

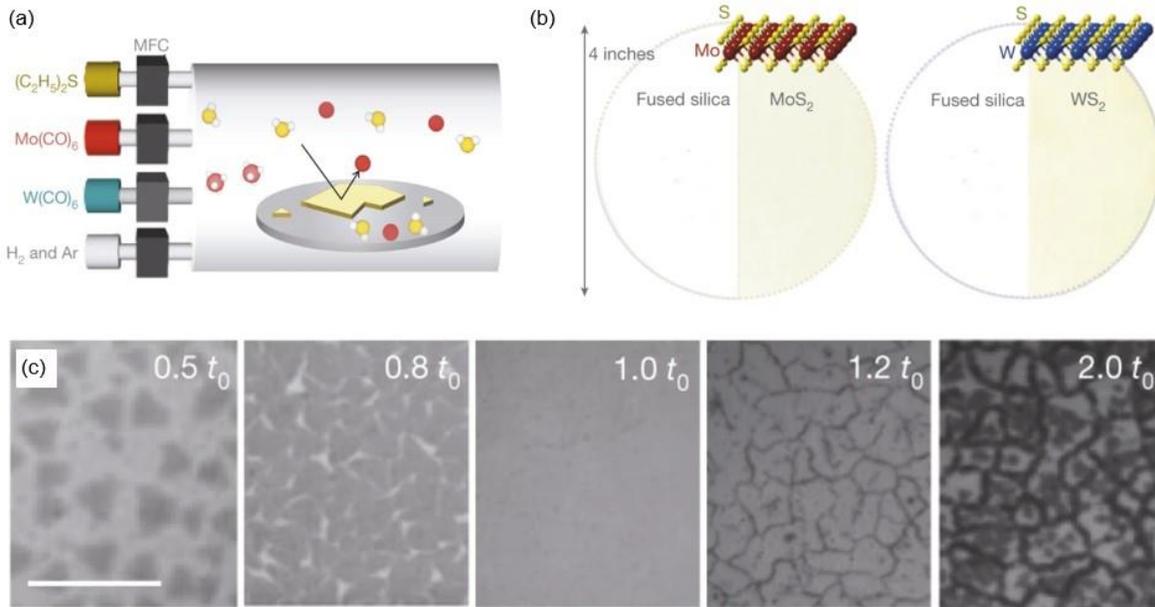


Figure 2.9 MOCVD growth of monolayer TMDs. (a) Schematic of MOCVD growth setup. (b) Photographs of monolayer MoS₂ (left) and WS₂ (right) films grown on 4-inch fused silica substrate. Left half of each wafer shows bare fused silica substrate for comparison. (c) Optical images of MOCVD-grown MoS₂ at different growth times, where t_0 is the optimal growth time for full monolayer coverage. Scale bar, 10 μm . Reproduced from Ref. 18.

maximum monolayer coverage (t_0), followed by nucleation mainly at grain boundaries ($1.2 t_0$) and bilayer growth ($2 t_0$). No nucleation of a second layer is observed until the full monolayer coverage over the substrate, resulting in an optimal growth time, t_0 . The high-quality, homogeneity and continuity of semiconducting MoS₂ and WS₂ films are confirmed using methods, such as optical microscopy, photoluminescence spectroscopy and electrical characterization of batch fabricated devices. From ~8100 MoS₂ FETs, a device yield of 99% was obtained and they exhibited a high room

temperature mobility of $\sim 30 \text{ cm}^2/\text{V}\cdot\text{s}$. This approach provides an ideal platform for generating monolayer TMDs on a technologically relevant scale. Therefore, TMD films grown by this method will be the source of materials for our work in this thesis, unless stated otherwise.

CHAPTER 3

FACTORS CONTROLLING ELECTRICAL TRANSPORT IN ATOMICALLY THIN TMDs

3.1 Introduction

In the previous chapter, we have looked at a few of the consequences that reduced dimensionality of TMDs can have on their electronic properties. Their all-surface nature gives us new degree of freedom to tune the states of electrons, spins, phonons, and so on. In relation to understanding their electrical transport, this means that the interactions of electrons can now be tuned based on what we put around their surfaces. This feature, in reality, can simultaneously be advantageous and a challenge. While in many cases we can modify the surface of the materials purposefully to tune their properties, in many other instances there are elements that unintentionally alter their properties and directly affect the final electrical measurements. It is worth noting that the unintentional perturbation can occur both during the growth and in the processes of device fabrication and measurements. This poses a practical challenge to predict and control the performance of a TMD-based device. In this chapter, the goal is to review the main factors that can influence the transport in TMD-based devices with the intention to give a better understanding of various contributions that might be in play when we measure a particular device behavior.

Figure 3.1 displays two categories of factors that can influence electronic properties of 2D materials: intrinsic factors formed during the growth and extrinsic factors introduced after the growth. The former includes zero-dimensional atomic defects such as vacancies, anti-sites, substitutions and one-dimensional defects such as edges and grain boundaries. While atomic defects can create scattering centers which can degrade the carrier mobility, they also provide ways to modify the carrier concentration of materials or create hopping centers for charge transport.

Substitutional doping is one of the effective ways to precisely tailor the electronic properties. Extrinsic factors, on the other hand, include strain, adsorbates, surface roughness, charged impurities in the substrate, and oxidation which can affect multiple properties by introducing charge scattering, electrostatic potential variation and modifying the band structure.

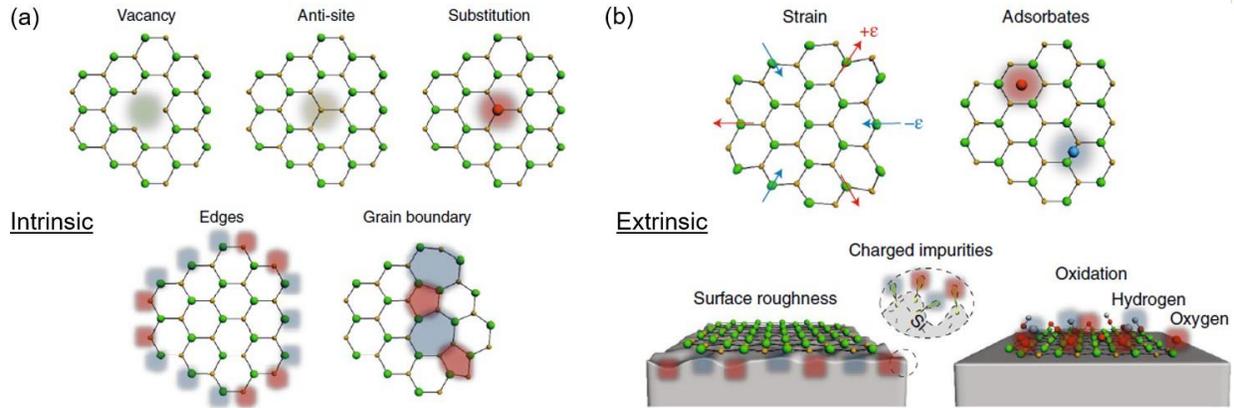


Figure 3.1 Factors that can influence electronic properties in 2D materials. (a) Intrinsic factors: vacancy, anti-site, substitution, edge termination and grain boundary. (b) Extrinsic factors: strain, adsorbates, surface roughness, charged impurities in the substrate, and oxidation. Reproduced from Ref. 46.

3.2 Defects and Substitutional Dopants

Defects

The defect density in starting TMD material can play a significant role in its transport behavior. For example, CVD-grown MoS₂ typically has much lower carrier mobility than mechanically exfoliated samples due to the structural disorders induced during the growth process such as vacancies and grain boundaries.⁴³ The most abundant point defects in TMDs are vacancies and antisites. Their role on electrical properties of TMDs, especially MoS₂ has been extensively researched.⁴⁷⁻⁵¹ It is believed that one of the main reasons why CVD-grown monolayer MoS₂ generally exhibits *n*-type conductivity is the presence of high-density sulfur vacancies ($\sim 10^{13}/\text{cm}^2$).⁴⁹ The commonly observed point defects⁴⁹ include mono- (V_s) or divalent (V_{S2}) sulfur

vacancies, varied complexes of Mo and nearby sulfur atoms (*e.g.*, complex of Mo and three sulfur, MoS₃), and antisite defects where a Mo atom substitutes a S₂ column (MoS₂) or a S₂ column substituting a Mo atom (S₂Mo). Under sulfur rich conditions, V_s has been found to have the lowest formation energy (~2 eV) and so is frequently observed experimentally.⁴⁷ As per one of the explanations, the V_s and V_{S2} result in the defect levels below conduction band minimum of MoS₂ (Figure 3.2a). These induced gap states bring the fermi level close to the conduction band minimum leading to *n*-type conductivity in MoS₂. Moreover, the presence of metallic defects in MoS₂ has been demonstrated to cause huge variations in the fermi level, as large as 1 eV.⁴⁸ Interestingly, both *n*-type and *p*-type conductivity of MoS₂ has been observed from different regions of the MoS₂ sample (Figure 3.2 b, c). While the *n*-type behavior is associated with sulfur

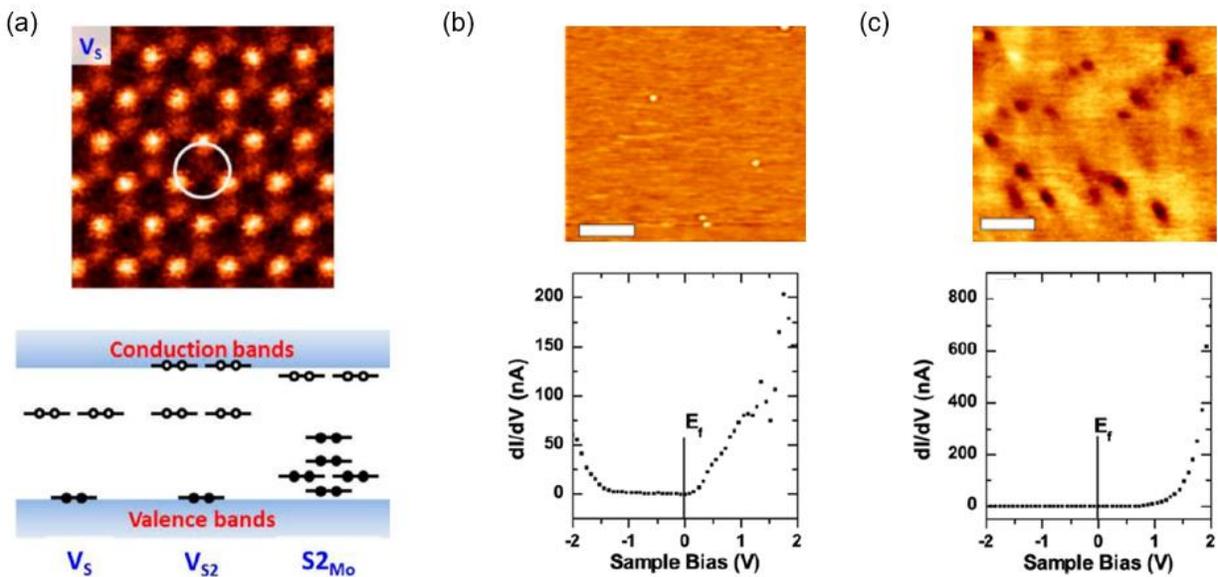


Figure 3.2 Intrinsic defects in MoS₂. (a) Atomic resolution annular dark field image of monosulfur vacancy, V_s (top) and schematic representation of the defect levels (bottom) in monolayer CVD MoS₂. (b) Scanning tunneling microscopy (STM) image of MoS₂ showing observed bright defects (top) and dI/dV measured by scanning tunneling spectroscopy (STS) acquired from same region showing the Fermi level close to the conduction band edge (bottom). (c) STM image with higher concentration of darker defects (top) and dI/dV measured by STS acquired from same region showing the Fermi level position more than 1 eV away from the conduction band edge (bottom). (a) is reproduced from Ref. 47 and (b), (c) from Ref. 48. STM scale bars are 20 nm.

vacancies, the p -type is associated with sulfur rich regions. There have been attempts to passivate the defect states from the gap and heal the sulfur vacancies using thiol-based chemistry and bis(trifluoromethane) sulfonimide (TFSI) superacid.^{51,52} These observations confirm that intrinsic defects strongly influence electrical properties in ways that are not precisely tunable.

Substitutional Dopants

In order to control the polarity of carriers and conductivity in TMDs, substitutional doping is one of the efficient ways. However, methods like ion-implantation which are used for bulk semiconductors for precise and localized doping cannot be used for TMDs due to their extreme susceptibility to damage. Alternatively, introduction of dopants in-situ during growth to substitute metal or chalcogen atoms is deemed to be effective for TMDs. For example, doping of atomically-thin MoS₂ and WS₂ monolayers with niobium (Nb) and rhenium (Re) atoms is a well-known strategy.^{53,54} Substitution of transition metal atoms (Mo or W) with Nb (Re) which has one less (more) d -electron leads to p -(n -) type doping of the TMDs. Assuming complete ionization, each Nb (Re) is expected to provide one additional hole (electron) into the material and increase the electrical conductivity. Figure 3.3a shows a representative result of the Nb doped WS₂ grown by CVD using powder precursors which has typical triangular grains of WS₂. This implies that the incorporation of the atoms does not introduce other structural and lattice defects. The analysis of atomic structure clearly shows different contrasts for W (brighter yellow) and Nb (dimmer purple) atoms confirming the replacement of some of the W atoms with the Nb atoms (Figure 3.3b). Similar studies have been conducted for Re-doped MoS₂.^{53,54} To look into the effect of Nb doping on electrical characteristics of MoS₂ FETs, an illustrative data set is shown in Figure 3.3c. It shows that the doped channel gives rise to a p -type conductivity in an otherwise n -type undoped MoS₂ due to degenerate hole doping.⁵⁵ Indeed, doping TMDs in such a way provides a knob to control

the polarity of carriers and thereby, facilitates electronic applications where a p - n junction or bipolar transport is required.

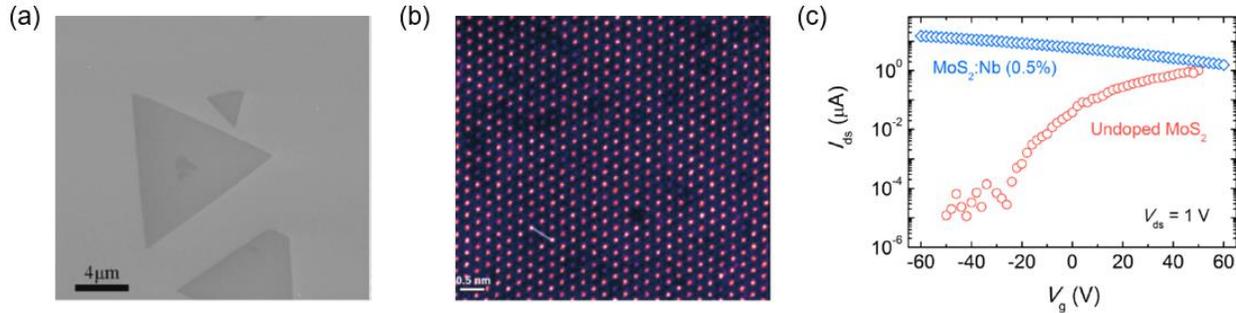


Figure 3.3 Substitutional doping in TMDs. (a) Scanning electron microscopy image of monolayer Nb-doped WS₂ triangular grains. (b) Aberration-corrected Z-contrast scanning tunneling electron microscopy image of monolayer Nb-doped WS₂. The yellow and purple dots represent W and Nb atoms, respectively. (c) Transfer curves from MoS₂:Nb and undoped MoS₂ FETs. (a), (b) have been reproduced from Ref. 53 and (c) from Ref. 55.

Another way to tune the electrical properties of TMDs is to introduce isoelectronic dopants which have the same number of valence electrons as the substituted atoms in the host materials. Isoelectronic dopants tend to form alloys more easily, impede generation of dislocations and reduce the formation of native defects.⁵⁶ Although isoelectronic dopants do not add electrons or holes, they can still lead to chemical and structural modifications in TMDs, and alter its band structure. Controlling the stoichiometric ratios of dopants to host atoms during the CVD growth has been shown to produce monolayers of TMD alloys, *e.g.*, Mo_{1-x}W_xSe₂, MoS_xSe_{2-x}, WS_xSe_{2-x} and Mo_xW_{1-x}S₂.⁵⁶⁻⁵⁹ A representative atomic structure of monolayer Mo_{0.82}W_{0.18}Se₂ metal alloy obtained using STEM is shown in Figure 3.4a, where few of the Mo sites with brighter contrast are occupied by W atoms. This confirms the successful substitution of Mo with W atoms without observation of any interstitial atom. The transfer characteristics of MoSe₂ and Mo_{1-x}W_xSe₂ FETs with varying W concentrations show that while monolayer MoSe₂ exhibits a n -type behavior,

$\text{Mo}_{0.82}\text{W}_{0.18}\text{Se}_2$ has a *p*-type behavior (Figure 3.4b). Increasing W doping clearly leads to a suppressed (enhanced) *n*-type (*p*-type) transport behavior. Furthermore, alloys where host chalcogen atoms are substituted have also been successfully grown. Figure 3.4d shows transfer curves of $\text{WS}_{2x}\text{Se}_{2-2x}$ nanosheet transistors with different S atomic ratios from nearly pure WSe_2 (brown curve) to nearly pure WS_2 (black curve). It suggests that for WSe_2 -rich alloys, FETs display a *p*-type behavior, while for WS_2 -rich alloys, the predominant transistor behavior is *n*-type, and the intermediate alloy region exhibits weak ambipolar behavior. One thing to note, however, is that the size of doped TMDs is still limited to a few micrometers (Figure 3.4c) and precise tuning of dopant concentrations hasn't been achieved.

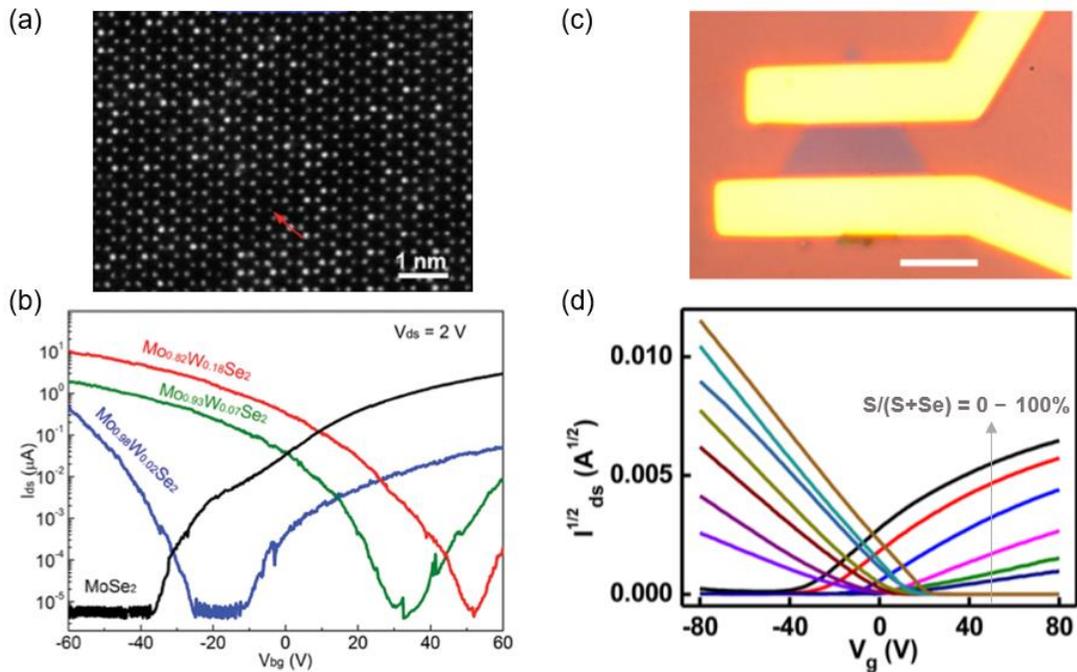


Figure 3.4 Alloying of TMDs. (a) Aberration-corrected Z-contrast STEM image of monolayer $\text{Mo}_{0.82}\text{W}_{0.18}\text{Se}_2$ alloy. Brighter spots correspond to sites where W substitutes Mo. (b) Transfer curves of FETs based on monolayer MoSe_2 and $\text{Mo}_{1-x}\text{W}_x\text{Se}_2$ with different W concentrations. (c) Optical image of a FET made of $\text{WS}_{2x}\text{Se}_{2-2x}$ nanosheet flake (scale bar is 5 μm). (d) Transfer curves of $\text{WS}_{2x}\text{Se}_{2-2x}$ FETs with different S atomic ratios, from nearly pure WSe_2 (brown curve) to nearly pure WS_2 (black curve). (a), (b) have been reproduced from Ref. 56 and (c), (d) from Ref. 58.

3.3. Carrier Scattering and Charge Transfer Doping

Beyond the intrinsic defects in TMDs, there are multiple extrinsic factors that can influence the conductance. For example, strain induced by the roughness of the substrate surface can strongly modify the local band structure leading to significant modulations in the band gap (1.23–2.65 eV). This variation in the local band structure can even result in a direct to indirect band gap transition.⁶⁰ In this section, we will focus on charge scattering and charge transfer doping in TMDs.

Carrier Scattering

The major sources of carrier scattering in 2D FETs are summarized in Figure 3.5a. It includes electron-phonon interactions, coulomb scattering from charged impurities (CIs), surface optical phonons (remote interfacial phonons), surface roughness, and structural defects. The electron-phonon scattering is an intrinsic scattering mechanism which often dominates at room temperature and therefore, the theoretically predicted phonon-limited mobility sets an upper limit for the experimentally achievable mobilities in monolayer MoS₂. The predicted phonon-limited mobility for monolayer of MoS₂ is $\sim 410 \text{ cm}^2/\text{V}\cdot\text{s}$, which is much higher than the experimentally observed values, indicating that other scattering mechanisms may play a significant role.⁶² A

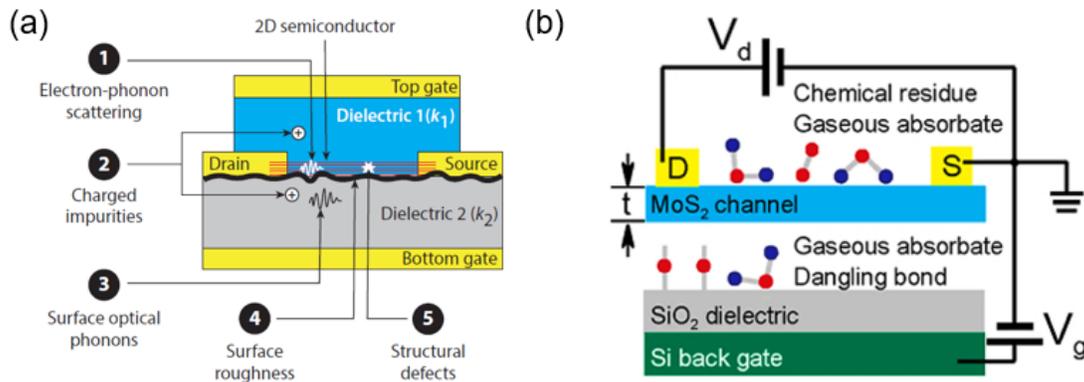


Figure 3.5 Charge scattering in 2D semiconductor FETs. (a) Schematic of 2D layered FET in dual gated geometry. (b) Schematic of charged impurities in a MoS₂ FET, located on top and bottom channel surfaces. (a) and (b) have reproduced from Ref. 61 and Ref. 63 respectively.

combined theoretical and experimental study indeed shows that the leading CIs scatterers in electrically gated FETs, *e.g.*, chemical residues, adsorbates on the top channel surface, and surface dangling bonds of gate dielectric on the bottom channel surface are more crucial for ultrathin channels.⁶³ The electron distributions and their average interaction distance from CIs (d) upon gating for mono- and few-layer thick channels show that in contrast to thicker channel, the carriers are squeezed into the monolayer which reduces d and thereby, increases the Coulomb scattering rate (Figure 3.6a). The shortened distances of carrier distribution peaks from top (d_t) and bottom surfaces (d_b) result in stronger interfacial scattering. The consequence of this is quite evident from the monotonic reduction in mobilities with number of layers for higher impurity density on both, top (n_t) and bottom surfaces (n_b) (Figure 3.6b). This confirms the extremely crucial role of CIs on either side of channel towards performance degradation of FETs, especially for monolayer TMD channels.

A common approach to suppress charged impurity scattering between carriers and CIs is by placing the TMDs in high- κ dielectric environments.^{61,64,65} For 2D crystals, most of the electric field between the carriers and impurities exists outside the 2D material, in the surrounding dielectric and so the main contribution to Coulomb interaction comes from the dielectric constant (ϵ) of the dielectric medium. The inverse relation of Coulomb interaction and dielectric constant justifies the damped scattering and improved carrier mobilities. This is unlike bulk semiconductors where the Coulomb interaction is dominated by bulk dielectric constant of the semiconductor itself. The response of devices on different dielectric oxides in Figure 3.6c (black: SiO₂, $\epsilon \sim 3.9$; green: Al₂O₃, $\epsilon \sim 10$; red: HfO₂, $\epsilon \sim 16.5$) shows that high- κ dielectrics help in increasing the mobility for samples with high impurity densities as transport in this regime is limited by impurity scattering. On the other hand, for cleaner samples with low impurity densities, low- κ dielectrics

can give higher mobilities relative to high- κ ones because the transport in this regime is limited by the remote phonon or surface optical phonon scattering which is suppressed for low- κ dielectrics. The significant variations between experimentally observed mobilities (few tens of $\text{cm}^2/\text{V}\cdot\text{s}$) and intrinsic phonon-limited mobility ($\sim 400 \text{ cm}^2/\text{V}\cdot\text{s}$) is often attributed to the impurity scattering.⁶² One way to avoid scattering on the bottom channel surface is by suspending the devices without the substrate support. While efficient, it is limited to low range of gate induced charge density and weak gate capacitance. Encapsulation of devices with *h*-BN or HfO_2 has been the most effective way in improving the mobilities of TMD FETs (Figure 3.6d).

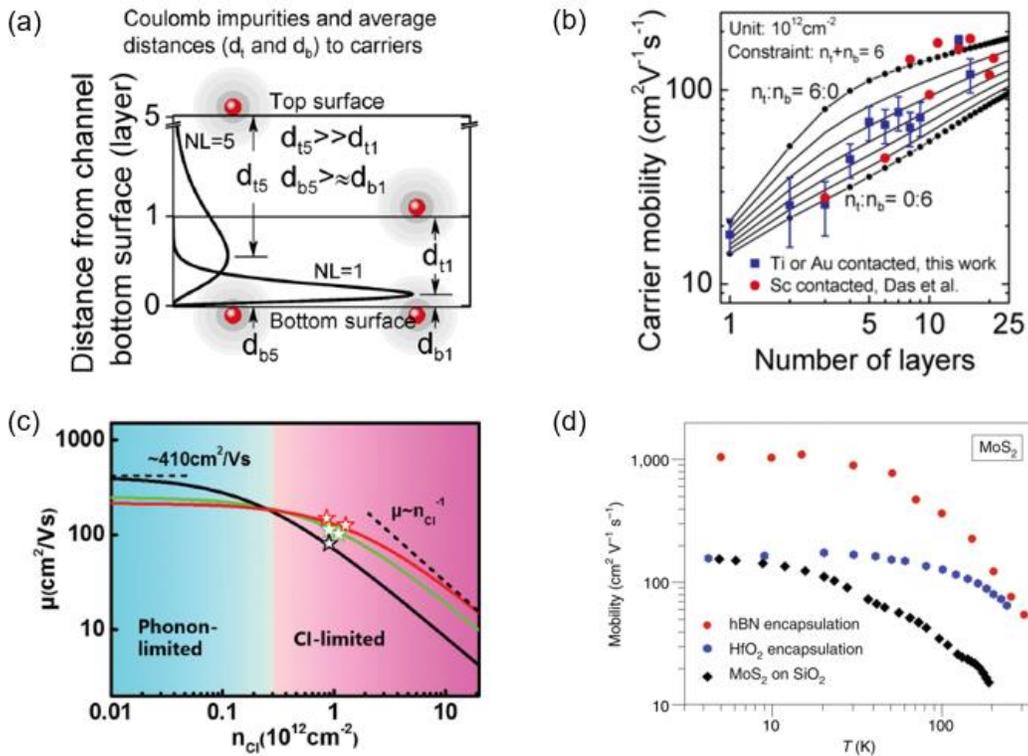


Figure 3.6 Effect of carrier scattering and ways to suppress it. (a) Comparison of interaction distances d_t and d_b between 1- and 5- layer channels. (b) Mobility vs thickness comparisons between calculation and experiment. (c) Predicted mobility as a function of impurity density, n_{CI} for devices on SiO_2 (black), Al_2O_3 (green), and HfO_2 (red). (d) Experimental observation of mobility vs temperature for monolayer MoS_2 on SiO_2 and encapsulated in HfO_2 , *h*-BN. (a), (b) reproduced from Ref. 63, (c) from Ref. 64 and (d) from Ref. 46.

Charge Transfer Doping

Another common strategy to tune the transport in TMD FETs is to use molecules or dopants with chemical potentials different than the semiconductor.^{10,66-69} The difference in the potentials leads to a direct redox reaction via charge transfer that alters the Fermi level. Molecules with strong reducing (oxidizing) nature can therefore, cause *n*-doping (*p*-doping) of TMDs. For example, benzyl viologen (BV) is an organic molecule with one of the lowest reduction potentials among the organic molecules. The energy diagram in Figure 3.7a shows the expected energy level offset between the conduction band edge of MoS₂ and the reduction potential of the BV molecule. MoS₂ has a conduction band edge at around 0 V with respect to the standard hydrogen electrode (SHE), while the reduction potentials of the BV molecule are lower. Due to this energy level offset, BV⁰ molecule can readily transfer electrons to MoS₂, which acts as an electron acceptor. The significant *n*-doping of MoS₂ by BV is confirmed by the higher on-current level in the doped device than that in the undoped one (Figure 3.7b). Besides, *n*-type doping of MoS₂ with other chemicals, *e.g.*, potassium vapor, dichloroethane and poly(ethyleneimine) has also been shown to increase the on-

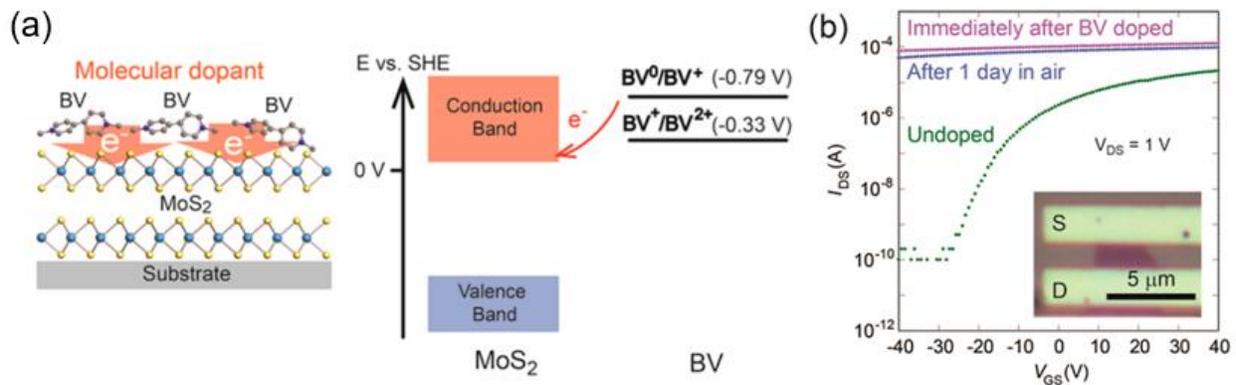


Figure 3.7 Charge transfer doping of MoS₂. (a) Schematic illustration of benzyl viologen (BV) surface doping of MoS₂ (left) and band diagram of MoS₂ and BV redox states. The conduction band edge of MoS₂ is located at ~ 0 V vs SHE, which is lower than the redox potentials of the BV molecules. This energy level offset leads to electron transfer from BV molecules to MoS₂. Reproduced from Ref. 66.

state current and decrease the contact resistance. Similar effect has been observed upon p -type doping of monolayer WSe₂ using oxidizing NO₂ molecules. The mechanism behind this improvement comes from reduction in the Schottky barrier widths at metal-semiconductor interface as we will see in the next section. While charge transfer doping is an effective knob for conductivity tuning, it is limited in terms of lack of precise control over doping levels and for many cases, lack of environmental stability because of exposure to air, high humidity or a high temperature.

3.4 Role of Injection Barriers at Semiconductor-Metal Contacts

The role of resistance at metal-semiconductor contacts and the carrier injection mechanisms on electrical performance of devices cannot be stressed enough. Before specifically discussing the contacts between metals and 2D semiconductors, we will briefly touch upon the band structure and the barrier that arise assuming an ideal case of contact with no interface states or anomalies. This has been well explained in Ref. 30.

We will consider two example cases, one for an intrinsic semiconductor (i -SC) and another for a n -type semiconductor (n -SC), both contacting the same metal, M . Before contact, the metal and semiconductors are two separate systems. The work function is the energy difference between the vacuum level and the Fermi level. For metal, it is denoted by $q\phi_m$, and for semiconductor it is given by $q\phi_s$ or $q(\chi + \phi_n)$, where q is the electronic charge, $q\chi$ is the electron affinity measured from conduction band minimum (CBM), E_C to vacuum level, and $q\phi_n$ is the energy difference between E_C and the Fermi level. The difference between the two work functions is called the contact potential and is given by $\phi_m - (\chi + \phi_n)$. In this example, this potential is close to zero for an i -SC ($\phi_m - \phi_s \sim 0$), while it has a finite value for a n -SC ($\phi_m - \phi_s > 0$). When the metal contacts the semiconductor, there is charge flow which is proportional to the contact potential and the direction

of flow is from the lower work function system to the higher work function system. This charge flow establishes thermal equilibrium as a single system and the Fermi levels on both sides line up. Relative to the metal's Fermi level, the Fermi level is lowered in the semiconductor by an amount equal to the difference between the two work functions as shown in Figure 3.8. A consequence of this is generation of a barrier for electrons, the height of which is given by $\phi_{Bn0} = q(\phi_m - \chi)$, also known as the Schottky barrier height (SBH). The SBH is dependent on the work function of metal and electron affinity of the semiconductor alone which implies that for both *i*-SC and *n*-SC, the value of SBH is the same. However, we see that for the latter where the Fermi level of semiconductor is closer to the CBM, there is larger band bending which results in a narrower depletion or Schottky barrier width, W facilitating better carrier injection compared to the former.

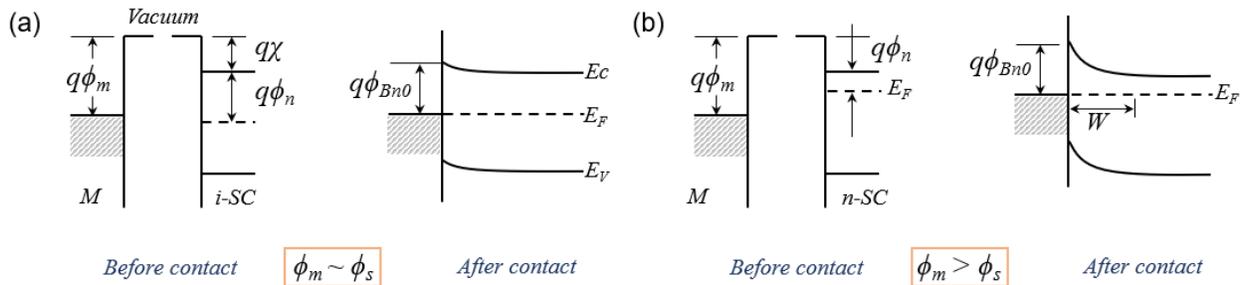


Figure 3.8 Energy band diagrams of metal-semiconductor contacts. (a) Metal and an intrinsic semiconductor in separated systems (left) and connected in one system (right). (b) Metal and a *n*-type semiconductor separated (left) and connected in one system (right).

In 2D FETs, due to their lack of dangling bonds, they tend to interact with metal via vdW forces unlike bulk semiconductors which form covalent bonds with the metal. This vdW gap acts as an additional tunnel barrier for carriers besides the inherent Schottky barrier (Figure 3.9).

The presence of Schottky barrier is unavoidable if the fermi level of metal lies within the band gap of semiconductor and is one of the key causes for high contact resistance in 2D FETs. There are two main approaches for producing low resistance contacts: (a) thinning the Schottky

barrier width by degenerately doping the contact regions, and (b) lowering the Schottky barrier height by selecting contact metal with high (for p -type semiconductors) or low (for n -type semiconductors) work function.

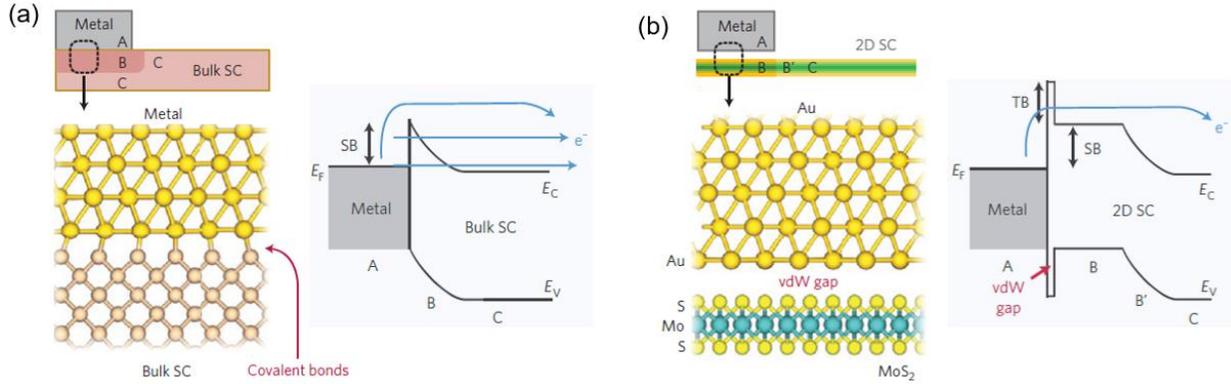


Figure 3.9 Different types of metal semiconductor junctions. (a) Schematic (left) and corresponding band diagram (right) of a typical metal/bulk semiconductor interface. The blue arrows represent different charge injection mechanisms. From top to bottom: thermionic emission, thermionic field emission and field emission (tunneling). (b) Schematic (left) and corresponding band diagram (right) of a metal/2D semiconductor interface with vdW gap. The arrow represents thermionic emission charge injection. This is assuming low doping level of semiconductor, say during electrostatic doping. Thermionic field emission starts to dominate as doping increases. Reproduced from Ref. 70.

One way to achieve the former is by using charge transfer to dope the semiconductor underneath the contacts as seen in the previous section. For the latter, while it seems straightforward to vary the SBH by choosing an appropriate metal contact, in reality, the chemical interactions between metal and semiconductor come into play and can frequently pin the Fermi level ceasing the one-to-one relation between metal work function and SBH. The most prominent consequences of such interactions during the typical processes of material integration and device fabrication are: (1) chemical disorders and defect-induced gap states (DIGS) that serve as a reservoir for electrons or holes and therefore, pin the Fermi level, and (2) metal-induced gap states (MIGS) formed in the junction owing to the decaying metallic wavefunction that penetrate to nanometer depth into the semiconductor and pin the Fermi level. In order to address the issue of

induced gap states, the main strategy has been to decouple the metal-semiconductor interaction by introducing a thin dielectric, molecular layer, or vdW gap at the interface.⁷¹⁻⁷³ The vdW integration of metal thin-film electrodes and 2D semiconductors by transfer of electrodes has been demonstrated to be a gentler and low-energy materials integration strategy compared to the conventional direct deposition of electrodes. The electron microscopy images in Figure 3.10a, b clearly show that while transferred metal/MoS₂ junctions are atomically sharp and clean, the deposited metal/MoS₂ junctions exhibit considerable defects.⁷¹ The absence of DIGS and suppression of MIGS in the transferred metal/MoS₂ junctions allows for tuning the SBH by using different metal work functions (Figure 3.10c). However, we should note that the study is conducted for multilayer flakes whose electronic properties can be very different from monolayer TMDs. Another approach to achieve vdW contacts between monolayer MoS₂ and metals is by using

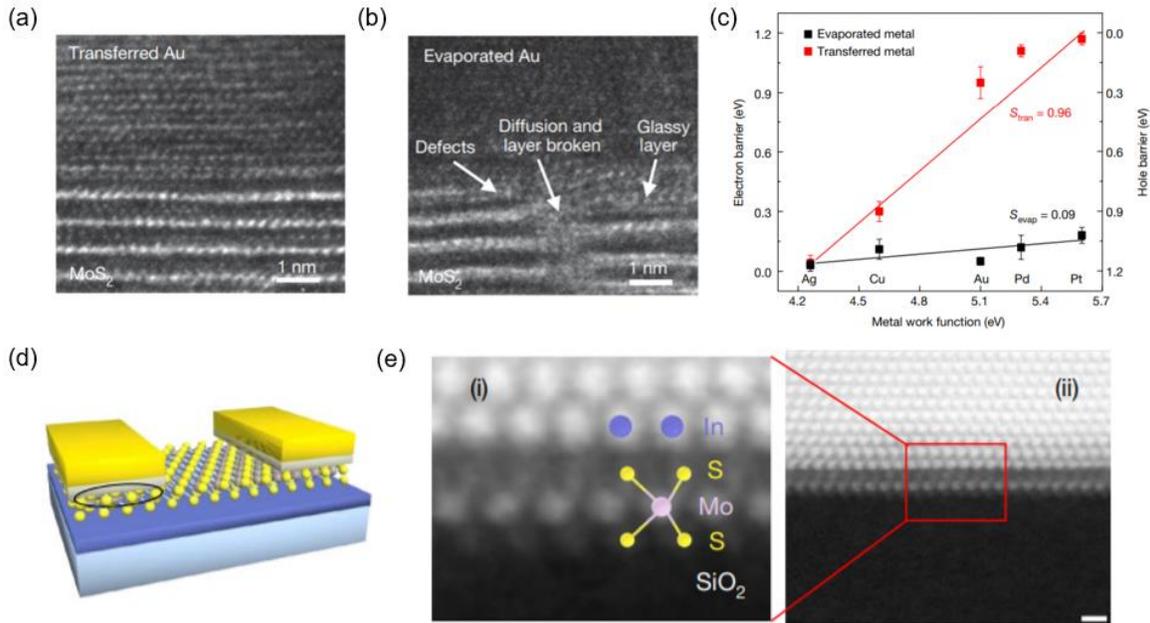


Figure 3.10 Strategies to form van der Waals gap at metal-2D semiconductor interface. (a), (b) Cross-sectional transmission electron microscopy images of transferred (a) and direct deposited (b) gold electrodes on multilayer MoS₂. (c) Schottky barrier height for transferred and evaporated metals. Reproduced from Ref. 71. (d) Schematic of bottom gate FET device structure with indium/gold alloy as electrodes. (e) Atomic resolution images of indium/gold on monolayer MoS₂ analyzed from under the contact as marked in (d). Scale bar, 5Å. Reproduced from Ref. 72.

indium/gold alloy as electrodes.⁷² It ensures formation of vdW gap at the atomically sharp, defect-free interface (Figure 3.10e).

In order to mitigate the MIGS, the use of semimetal-semiconductor contacts has recently been shown to avoid the gap-state pinning.⁷³ In comparison to the original density of states (DOS) of the semiconductor before contact (Figure 3.11a), after the contact of metal, the extended wavefunction from metal perturbs the semiconductor environment and leads to rehybridizations of semiconductor's original wavefunctions resulting in MIGS within the bandgap (Figure 3.11b). In this case, a Schottky barrier is inevitable due to the presence of Fermi level of the system within the semiconductor's band gap (Figure 3.11c). However, a semimetal like bismuth with nearly zero

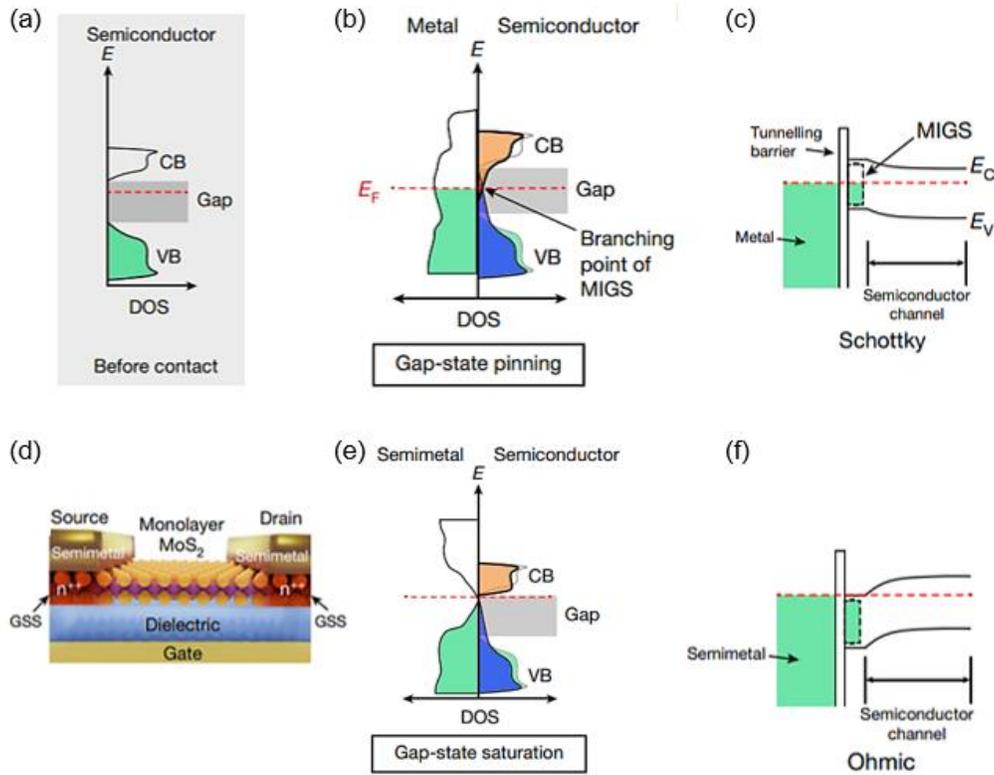


Figure 3.11 Concept of gap-state saturation at semimetal-semiconductor contact. (a) DOS of semiconductor before contact. (b) DOS of normal metal-semiconductor contact. (c) Band structure of metal-semiconductor contact. (d) Schematic of 2D FET with monolayer MoS₂ channel and bismuth semimetal contacts. (e) DOS of semimetal and semiconductor contact. (f) Band structure of semimetal-semiconductor contact. Reproduced from Ref. 73.

DOS at the Fermi level can greatly suppress conduction band contributed MIGS and lead to gap-state saturation of valence band (Figure 3.11e). This avoids any Schottky barrier at the metal-semiconductor interface (Figure 3.11f). A schematic of a FET device with bismuth contacts is shown in Figure 3.11d. Using this approach, an exceptionally low contact resistance of $123 \Omega \cdot \mu\text{m}$ for monolayer TMD FETs has been achieved, the lowest yet.

3.5 Summary

In this chapter, we discussed the main factors that can affect the electrical transport in monolayer TMD FETs. These factors can come into picture at different points until device completion, starting from the growth of monolayer TMDs itself. During growth, defects and dopants can be introduced which can tune their properties. After the growth, charge scattering comes into play *e.g.*, from the substrate, and the charged impurities can affect the device behavior. High k -dielectric oxides can then be deposited on the TMD surface to suppress them. Furthermore, one can tune the conductivity of TMDs by charge transfer using molecular doping techniques. The chemical doping methods can effectively reduce the barrier width at the contacts and increase the overall on-state conductivity of the devices. Such doping effects on monolayer MoS₂ due to solvent exposure will also be discussed in Chapter 5.

CHAPTER 4

ELECTRICAL MEASUREMENT APPROACHES FOR SEMICONDUCTING TMDs

4.1 Introduction

Until now, we have mentioned about the significant role of starting material properties and various other factors towards the electrical properties of TMD-based FETs. Due to the surface-sensitive nature of the TMD materials, the measurement of their electrical properties has become a new challenge which doesn't exist in bulk semiconductors. As previously mentioned in Chapter 1, the predominant measurement methods for monolayer TMDs are based on photo- and electron-beam lithography processes and involve steps that expose the surface of TMDs to multiple chemicals, UV or electron beam, heat and high energy metal atoms when defining contacts, all of which can potentially alter the properties of the pristine materials. Therefore, the act of measurements in these methods actually will change the outcome of the measurements.

To achieve predictable and controllable performance of TMD-based devices, a non-perturbative method for performing electrical measurements is needed with the following characteristics. First, the method should use a patterning approach that does not affect the surface of the material or device. Second, the electrical contacts need to be introduced gently to minimize any thermal, mechanical, and chemical damage to the device. Third, the method should be scalable to produce many devices for generation of statistically meaningful data. Lastly, it should be flexible enough to be used at any step of the device fabrication process. Such an approach would enable one to electrically probe atomically thin materials along the device fabrication process, all the way from growth to completion of the final devices. To date, there currently exists no such approach. In this chapter, we will discuss our non-perturbative measurement approach that allows us to define the two main elements of a monolayer TMD FET with minimum perturbations: the

active semiconductor channel and metal contacts. Prior to that, we will first briefly review the limitations of existing lithography-based measurement approaches and previous efforts made to address them.

4.2 Limitations of Existing Measurement Methods and Attempts to Address them

Electron-beam lithography (EBL) is one of the prominent fabrication techniques adopted for atomically thin materials, including exfoliated micrometer-scale samples.^{5,9-13,28,34,67,73} With the progress in the large scale synthesis of 2D crystals (tens of micrometers or larger) via CVD, photolithography has also become a mainstream measurement approach for 2D materials.^{17,24,43} Both methods involve steps that include spincoating of a polymer resist (electron beam sensitive for EBL and UV sensitive for photolithography) on top of the material, resist exposure to e-beam or UV light followed by its development in chemical developers and at the end, lift-off of polymers in solvents (Figure 4.1). In addition, metal contacts are usually directly deposited during which high energy metal atoms bombard on and coat the TMD surface. This process can cause local heating and can damage the crystal lattice at the metal-semiconductor interfaces as has been observed before.^{71,74}

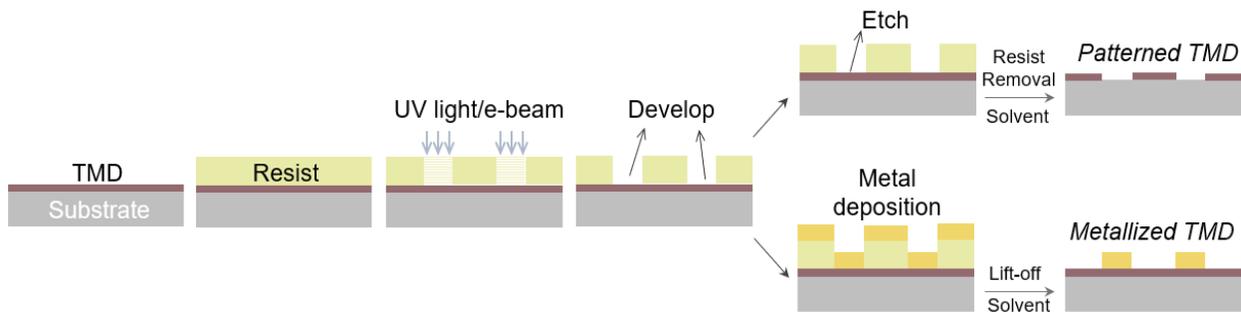


Figure 4.1 Steps involved in conventional lithography-based measurement. Schematic of a typical lithography process. It proceeds by coating a polymer resist and then introducing chemical change by exposing it to UV light or e-beam. The resist is then developed in a chemical developer. Following this, an etching of TMD can simply pattern it or a metal deposition and its lift-off in solvent can metallize it. By doing both, channels and contacts can be defined.

The lithography-based measurements to probe the atomically-thin materials can have quite a few limitations. The various studies done on TMDs, *e.g.*, charge transfer, substitutional doping, and effects of different chemicals, such as solvents and resists, rely on the lithography-based

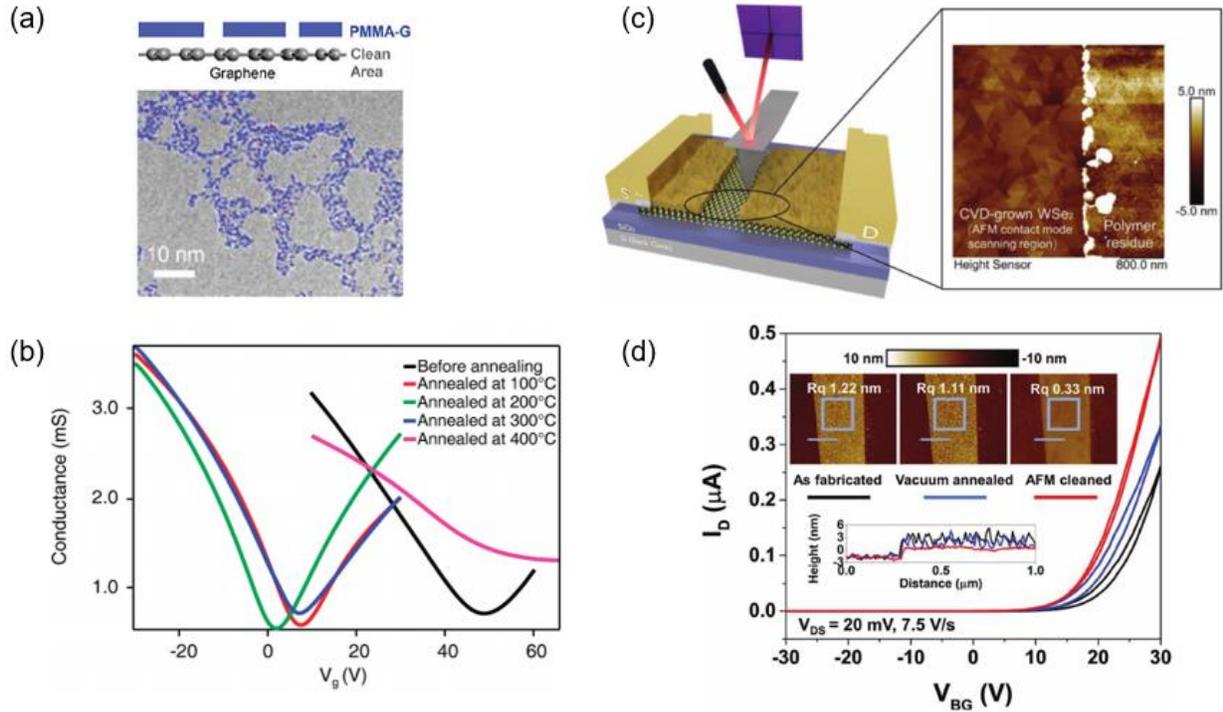


Figure 4.2 Unintentional effects of residues in 2D materials and ways to resolve them. (a) Transmission electron microscopy image of graphene after air and H₂/Ar annealing, post-lithography shows the PMMA residues. (b) Effects of thermal annealing on electrical properties of graphene. (c) Schematic of AFM contact mode cleaning and on the right, AFM image of a partially cleaned, CVD-grown WSe₂ with post lithography polymer residue. (d) Transfer curves and AFM images of a back-gated WSe₂ FET: as-fabricated, after vacuum anneal and after AFM cleaning. Inset shows line scans measured along the lines marked in AFM images. (a) has been reproduced from Ref. 80, (b) from Ref. 81 and (c), (d) from Ref. 76.

measurements.^{10,55,66-68,75,76} However, the materials in these studies were already exposed to resists, developers, etc. during the device fabrication process. This makes it extremely difficult to deconvolute the contribution of the variable being studied from the contribution of the measurement itself. Besides, contamination in the form of polymer residues on the material surface has been frequently observed for both graphene and TMD films. There have been more extensive

studies for graphene than TMDs to determine the role of these residues. It is believed that they can unintentionally dope the materials and can also degrade their electrical properties.⁷⁷⁻⁷⁹ For example, poly-methyl methacrylate (PMMA) resist residues have been found to cause a *p*-type doping in graphene. In attempts to minimize the effect of such extrinsic doping, methods like annealing in vacuum, Ar/H₂ environment or using current, and laser-based methods have been employed.⁷⁹⁻⁸⁴ Figure 4.2a shows the remaining PMMA residues on graphene after Ar/H₂ annealing at 250°C, implying that the annealing was not fully effective in getting rid of the residues. The shift in the Dirac point of graphene when annealed at different temperatures further suggests the variations lithography and post-fabrication processing can cause in the device behavior (Figure 4.2b). Even for TMDs, it has been proposed that residues can be *p*-type dopants. Contact mode atomic force microscopy (AFM) technique was used to clean the residues off of the surface (Figure 4.2c, d).⁷⁶ However, this method was not scalable. To summarize, all of these post-fabrication methods have mostly studied and tried to suppress the resist effect without considering the various other steps that are carried out during the device fabrication. Moreover, there is a finite probability that they themselves can induce changes in the structure and electronic properties of atomically-thin films and thus, act as additional contributors to the final measured device behaviors. As a result, lithography-based measurements result in a wide range of electrical characteristics of TMD-based devices.^{8,34,85,86} Even for monolayer MoS₂ (or WS₂) grown from similar conditions, considerable device-to-device variation in the mobility and contact resistance of the devices has been observed (Figure 4.3).⁸⁶ Hence, lithography-based device fabrication cannot provide accurate results as the lithography process itself affects the measured outcome.

In the last few years, there have been increased efforts to avoid conventional lithography altogether and adopt unconventional ways of electrical measurements. One such approach is to transfer the pre-patterned gold electrodes onto the few-layer TMD flakes using a PDMS support (Figure 4.4 a, b).¹⁵ This is to ensure a vdW gap and minimize strong interactions between the metal and channel as mentioned in the previous chapter. These devices are made such that the channel is encapsulated with PMMA on both its sides. It is believed that PMMA acts like a dielectric and reduces trap states. However, there are a few limitations of this method. First, it has been used to make devices with only thicker MoS₂ (> 4 nm thick) channels. The electrical properties of monolayer TMDs have not been probed. Besides, the random shapes and sizes of flakes imply that a fine control of the dimensions of channel lengths and widths is missing. This method is also limited in terms of its applicability for batch fabrication of pristine monolayer TMD-based devices. This is because of the lack of abilities to grow large-scale monolayer TMDs and pattern them with minimum perturbations. And finally, the presence of PMMA on both sides of channel means that there is at least one polymer or variable that the TMD already sees when it is electrically measured.

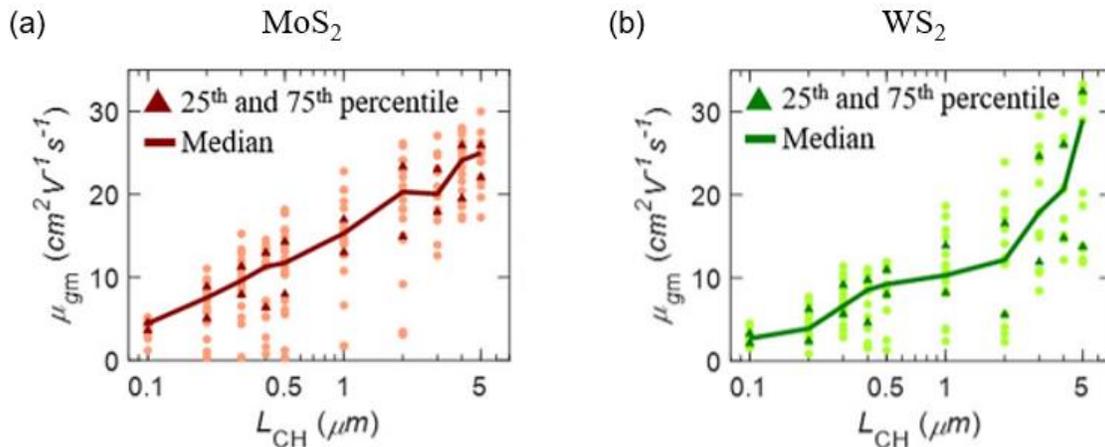


Figure 4.3 Device-to-device variation in mobility of MoS₂ and WSe₂ FETs. Distribution of mobility extracted for different channel lengths for (a) MoS₂ and (b) WSe₂ FETs. Shown are the median values of mobility and also 25th and 75th percentile values of distribution. Reproduced from Ref. 86.

This implies that the measured properties might still not entirely be of the pristine starting material as the role of PMMA towards the observed behavior cannot be quantified.

Another approach to avoid lithography for device fabrication involves a combination of patterned growth of 2D materials using a mask followed by direct shadow evaporation of metal electrodes (Figure 4.4c). As can be seen from the optical image of a typical device, the size of the mask used for patterned growth determines the scale of the channel, which in this case is $\sim 500 \mu\text{m}$. Since there exists no proper definition of channel between the metal electrodes, this means that there can be multiple pathways the current can travel through. Moreover, the use of direct deposition of metal can damage the crystal lattice as previously discussed.

Finally, scanning probe methods using conductive probes have been used to directly measure their properties and to study the effect of solvents. But, they are limited in terms of the

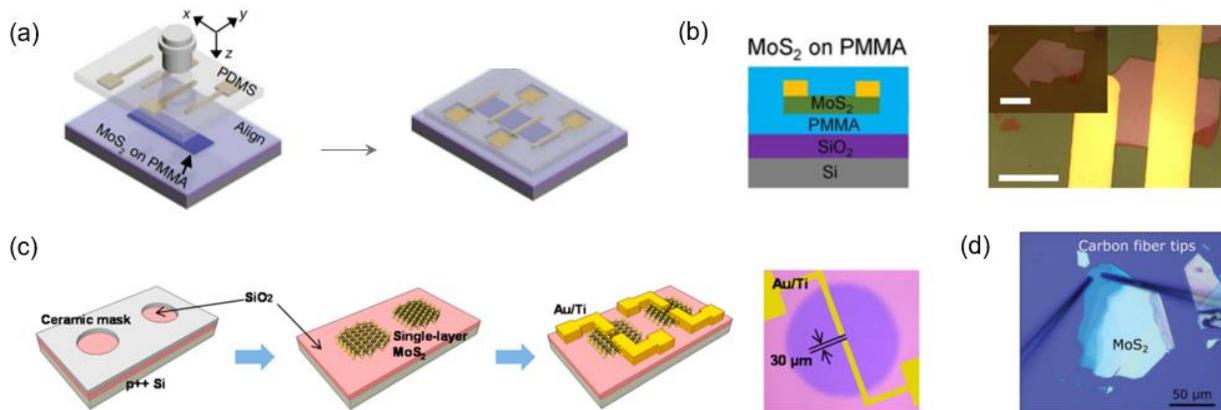


Figure 4.4 Unconventional approaches to measure the electrical properties of TMDs. (a) Schematic illustration of vdW integration of metal-semiconductor junctions. It shows the transfer of pre-patterned gold electrodes with PMMA atop on MoS₂ (left) that is followed by opening of PMMA windows (right). (b) A cross-sectional schematic of a MoS₂ FET enclosed with PMMA on both sides (left) and an optical image of ~ 15 layers MoS₂ flake on PMMA substrate with transferred platinum electrodes. Scale bar, 20 μm . (c) Schematic illustration of monolayer MoS₂ based FET fabrication involving patterned growth via CVD and shadow evaporation of metals. An optical image of a completed device (right). (d) Optical microscopy image of two carbon fiber tips contacting a MoS₂ flake. (a), (b) reproduced from Ref. 15, (c) from 87 and (d) from 88.

scale of measurements and therefore, the spatial uniformity of an observed behavior has not been evaluated.⁸⁷⁻⁸⁹ Thus, an approach of making TMD based FETs that meets all the criteria mentioned earlier in the introduction is still lacking.

4.3 Non-Perturbative Electrical Measurement Approach for Monolayer TMDs

In this section, we will introduce a non-perturbative method for performing electrical measurements of atomically thin materials with all the characteristics stated in the introduction of the chapter. It is based on a laser-patterning technique that directly defines conductance channels, while keeping the surface pristine, and a direct transfer of pre-made metal electrodes that minimizes damage to the material. Both processes can be carried out over a large scale. When applied to wafer-scale materials and devices, this method allows for the measurement of many devices for statistical analysis. Parts of this section have been written based on a manuscript which has been submitted (Ref. 90).

4.3.1 Laser-Assisted Non-Perturbative Patterning

The direct laser patterning of monolayer TMDs is conducted by raster scanning a focused laser beam (532 nm Q-switched pulsed laser) with controlled power and position to selectively remove the exposed film areas as illustrated in Figure 4.5a (See Appendix at the end of this chapter for details). The removal is mainly caused by the absorption of the laser leading to thermal ablation.⁹¹ Monolayer TMDs have up to 10% absorbance at ~2.3 eV photon energy corresponding to the specific wavelength²⁴ which allows them to be patterned in this way. This technique is effective for patterning other light-absorbing materials, such as metal thin films (Figure A4.1 of

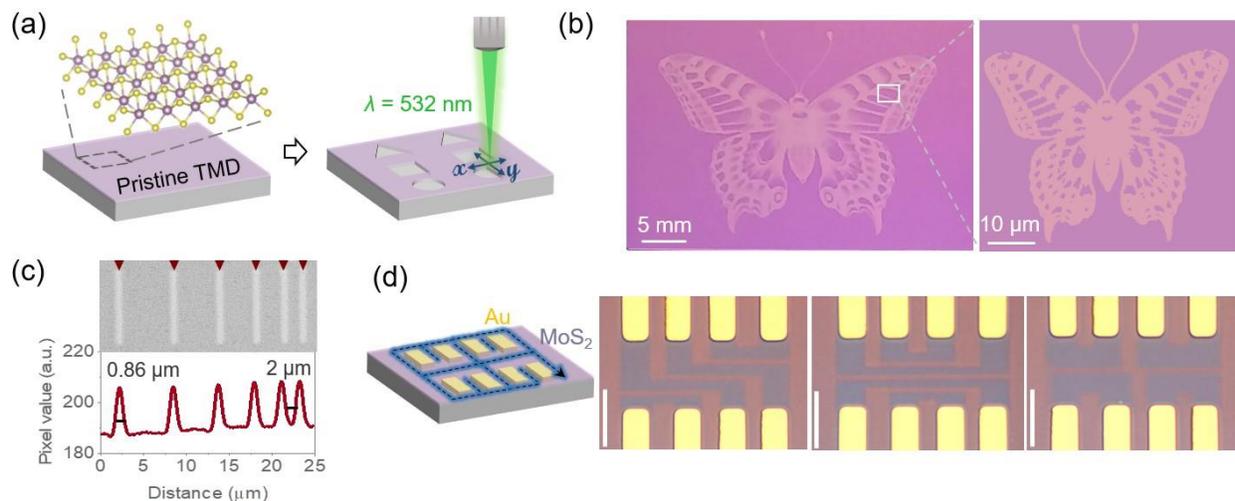


Figure 4.5 Non-perturbative, scalable, high-resolution patterning of TMDs. (a) Schematic of laser-based patterning of pristine as-grown monolayer TMDs using a Q-switched 532 nm laser. (b) Photograph of large-scale patterned (left) and optical micrograph of small-scale patterned (right) monolayer MoS₂. The areas with lighter color have been laser-ablated. (c) Optical micrograph of laser-patterned MoS₂ (top) and corresponding line profiles (bottom) extracted from the image. (d) Schematic of the laser patterning of MoS₂ after making electrode contacts (left) and optical images of three different designs of MoS₂ channels using similar sets of eight gold electrodes (right). Scale bars are 10 μ m.

Appendix). We note that the power of the laser needs to be carefully optimized based on a power-dependent assay (Figure A4.2) to selectively pattern each material without damaging the underlying substrate (for example, SiO₂/Si in our experiment). This is important to avoid gate leakage when measuring the devices.

Figure 4.5b shows two examples of monolayer MoS₂ on SiO₂/Si, each patterned following the same butterfly design over two different length scales (left: 1-inch, right: 50 μ m). This demonstrates that, depending on the choice of optical elements and magnification, the laser patterning can enable wafer-scale processing, as demonstrated for a 2-inch wafer (Figure A4.3), and can produce microscopic structures with a diffraction-limited spatial resolution. Figure 4.5c studies the spatial resolution of the laser patterning, where multiple lines were drawn with varying spacings (2 ~ 6 μ m) (top). The extracted line profile (bottom) shows a full-width-half-maximum

of $0.86 \pm 0.02 \mu\text{m}$ and clearly resolves the two lines with a $2 \mu\text{m}$ spacing. The laser patterning can be done before or after the electrode contacts. Performing the laser patterning in the presence of electrodes provides the flexibility of defining different microscopic conductance channels between similar sets of metal electrodes as shown in Figure 4.5d.

Importantly, the patterning ensures that the untouched areas of the TMD films remain unaffected such that their pristine, as-grown properties are preserved. This is supported by the characterizations done on patterned monolayer MoS_2 using photoluminescence (PL) spectroscopy and X-ray photoelectron spectroscopy (XPS). The PL measurements are performed using a confocal microscope with a 532 nm excitation laser under ambient conditions. Figure 4.6a compares the PL spectra acquired on, (i) as-grown MoS_2 film, (ii) remaining MoS_2 areas after conventional photolithography-based patterning and (iii) remaining MoS_2 areas after laser

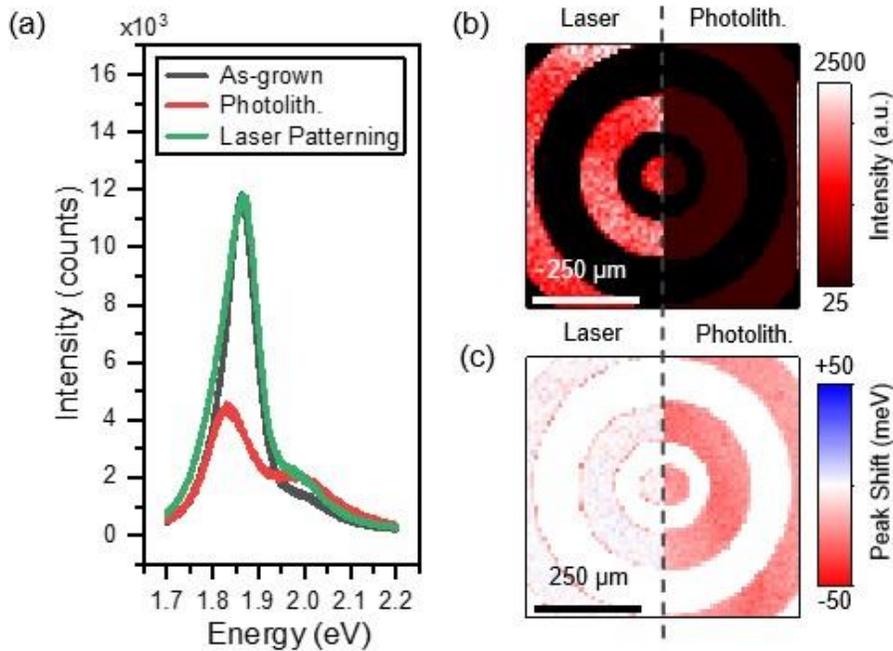


Figure 4.6 Photoluminescence spectroscopy of laser patterned samples. (a) Photoluminescence spectra acquired on as-grown MoS_2 film, intact MoS_2 areas after photolithography and laser patterning. (b, c) Comparison between photoluminescence maps for photolithographically- and laser-patterned samples: (b) peak intensity and (c) peak shift (relative to as-grown sample).

patterning. The samples for all three are from the same batch of grown MoS₂ for consistent comparison. While the PL intensity and principal line shape of laser patterned MoS₂ essentially remains same as that of as-grown MoS₂, the photolithography sample results in a significant decrease in intensity. The latter also shows a red shift relative to as-grown MoS₂ peak. To determine the spatial dependence of this observation, we performed PL mapping over a 500 × 500 μm² area centered on a bullseye pattern produced using laser and conventional photolithography (Figure 4.6b, c). These curves were fit by a simple gaussian model, resulting in maps of PL intensity and peak shift which have been overlaid for comparison. It shows that both reduction in PL intensity and red shift in the peak from remaining areas of MoS₂ after photolithography processing are spatially uniform. These observations clearly imply that laser patterning is non-perturbative and does not bring modification to the material's optical properties.

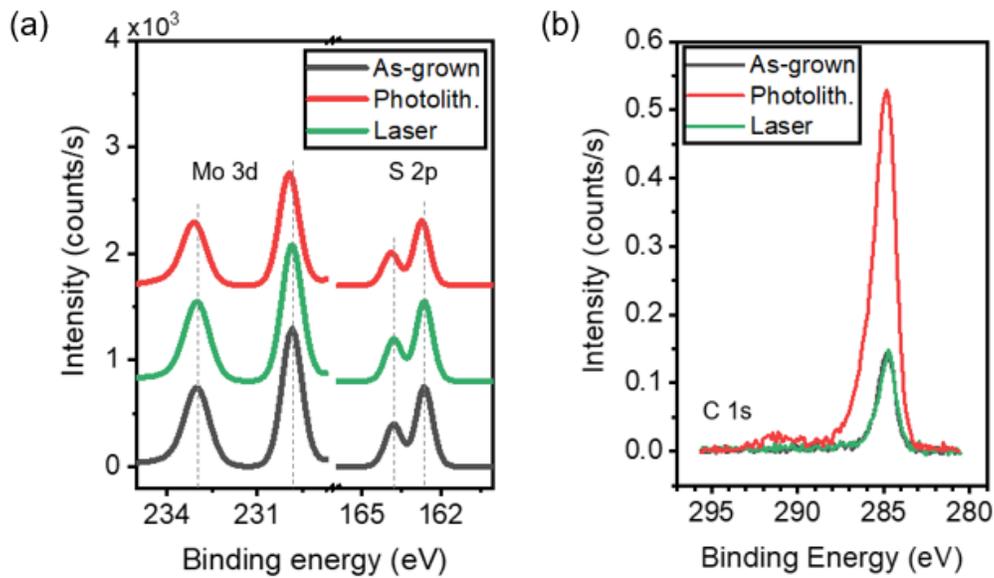


Figure 4.7 X-ray Photoelectron Spectroscopy of laser patterned samples. X-ray photoelectron spectra of: (a) Mo 3d and S 2p core levels, demonstrating nominal MoS₂ stoichiometry and negligible deviation between samples for different patterning techniques, (b) C 1s core level, showing increased carbonaceous contamination from polymer-based processing versus no increase from laser patterning.

Figure 4.7 shows the XPS results from remaining MoS₂ regions after patterning by different methods. The Mo 3d and S 2p core level spectra from photolithography patterned MoS₂ samples show a shift towards higher binding energies by 0.2-0.3 eV when compared to that of laser patterned and as-grown MoS₂. The upshift of binding energies is often attributed to a Fermi level shift towards the conduction band edge of the semiconductor and suggests a *n*-doping.^{92,93} The data, therefore, suggests that the MoS₂ is getting *n*-doped during the photolithography process. Besides, the spectra for as-grown and laser patterned MoS₂ overlap with each other and imply that MoS₂ after laser patterning remains chemically same as the as-grown state. Moreover, the C 1s core level spectra (Figure 4.7b) which is normalized to the Mo 3d peak show that the concentration of carbon present on the surface is almost double for photolithography patterned samples compared to that of as-grown and laser patterned samples. This suggests that while photolithography involving solvents and polymers leads to significant carbon contamination, laser patterning leaves the as-grown MoS₂ in an unaltered state.

4.3.2 Non-perturbative Electrode Transfer for Electrical Contacts

Figure 4.8a shows the schematic of the direct transfer of metal contacts and how this is used for non-perturbative electrical measurements. Our transfer method has two advantages over the conventional lithography approach: (1) it avoids hot metal deposition that can damage the TMD films, and (2) it keeps the TMD channel free of any polymer contact. To do this, (i) we start with an as-grown wafer-scale MoS₂ monolayer film with an array of large metal pads (deposited via shadow evaporation), which are used for probing only. The MoS₂ is then patterned using the laser to make conductive channels aligned to the metal pads. (ii) To make the actual electrical contacts to MoS₂, gold electrode/polymer spacer bilayers are fabricated on a separate substrate by

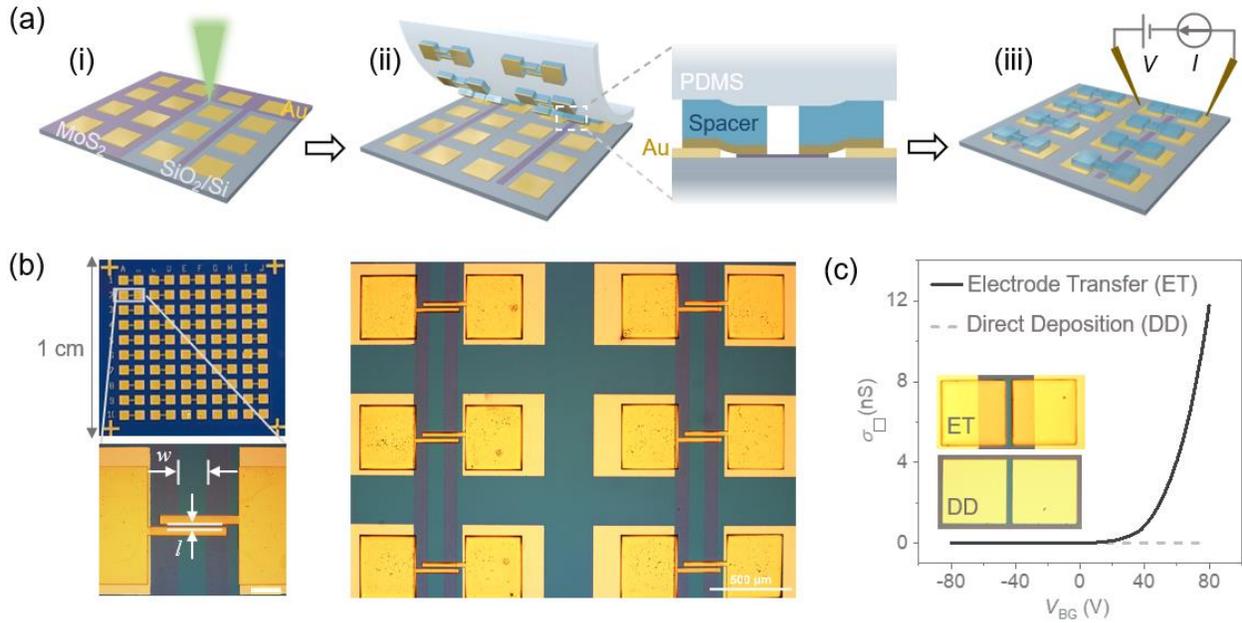


Figure 4.8 Non-perturbative electrical measurements of as-grown TMDs. (a) Schematic illustrating the non-perturbative measurement process. (b) Left: Photograph of a transferred electrode array onto MoS₂ channels, with magnified optical image of a transferred electrodes pair. Scale bar is 100 μm . Right: Slightly enlarged image of the device array showing 6 MoS₂ FETs (c) Representative transfer curves for MoS₂ channels, with contacts defined via electrode transfer (ET) and direct deposition (DD). Inset: Photographs of two devices fabricated using ET and DD of electrodes with the same aspect ratio. The size of the square pad is 110 \times 110 μm .

photolithography and transferred onto the MoS₂ film using a polydimethylsiloxane (PDMS) stamp. The purpose of the polymer spacers (1–10 μm thick) on top of the gold electrodes is to avoid direct contact between the PDMS and the surface of the MoS₂ (see the schematic of the cross-section in Figure 4.8a (ii) and optical images in Figure 4.9). Release of the PDMS stamp by gentle heating completes our process for fabricating the electrodes. The transfer of the electrodes completes the setup for non-perturbative conductance measurements, which are conducted under ambient conditions on a probe station using Si substrate as a back gate (iii). Figure 4.8b shows an optical image of a completed electrode array made using this process over a centimeter length scale (top left) and a magnified image of a pair of transferred electrodes (bottom left; with transparent spacer layers). We note that the channel width (w) is defined by the laser patterning and the channel length

(l) by the transferred electrode design. The details of the entire process are included in the Methods section in Appendix.

The electrodes transferred in this way make better electrical contacts to the MoS₂ as shown in Figure 4.8c. For this comparison, two sets of MoS₂ channels with the same dimensions ($l \sim 11 \mu\text{m}$ and $w \sim 117 \mu\text{m}$) are made using the laser patterning method. The only difference between them is how the contacts are made; for one, the gold contacts are defined using our non-perturbative electrode transfer, while for the other direct shadow evaporation is used. Only the devices made with transferred electrodes turn on at positive backgate voltage (V_{BG}), showing finite sheet conductivity (σ_{\square}). The result confirms that our transferred electrodes result in lower contact resistances compared to those of directly deposited ones. This is consistent with previous reports which show that direct deposition of metal contacts can damage TMDs.^{15,16}

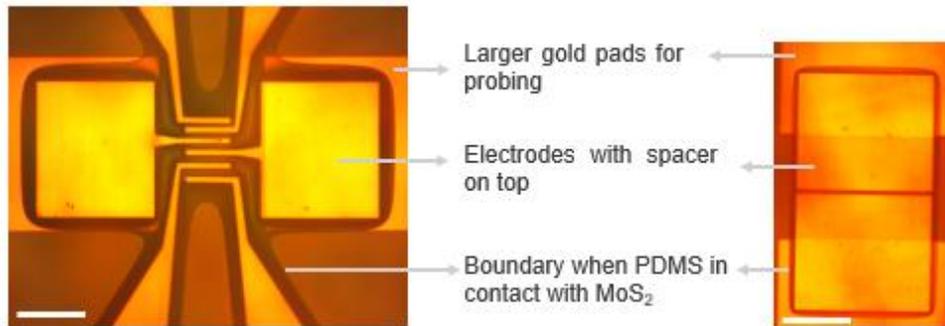


Figure 4.9 Preservation of as-grown MoS₂ surface during electrode transfer. Optical images during transfer of gold electrodes onto MoS₂ channels. Left: Transferred electrodes designed for channel length measurement; Right: electrodes designed for two-probe measurement. Scale bar for both: 200 μm . Shown are larger gold pads for probing, transferred electrodes with polymer spacer on top and the boundary when PDMS is in contact with MoS₂. The visible boundary confirms that PDMS does not touch the channel regions and therefore, keeps the channel pristine.

4.4 Summary

In this chapter, we have discussed an approach to define the channels and electrical contacts of monolayer TMD-based FETs, simultaneously over a large scale while avoiding chemical, mechanical and thermal damage to the TMD surface. The method is based on a combination of

direct laser patterning and electrode transfer methods. Moreover, this method is scalable and it enables us to batch fabricate many devices for statistical analysis of electrical data. This technique addresses the prior limitations of the existing lithography-based electrical measurement approaches which can cause unintentional doping and variations in the electrical properties of these materials. Our method can be used as a tool for precise tuning of electronic properties of monolayer TMDs.

4.5 Appendix

Methods

Non-perturbative laser patterning. Wafer scale monolayers of TMDs are grown via MOCVD¹⁸. Laser patterning is done in an ambient environment using a 532 nm pulsed yttrium orthovanadate (YVO₄) Q-switched laser integrated in a commercial system (Keyence MDT-1010W Telecentric Laser Marker). The laser operates via a Q-switching mechanism that allows generation of short high energy pulses.⁹⁴ It has a maximum average power of 4 W and pulse duration of ~100s of nanoseconds. The average and peak laser powers vary with a given set of input laser power (in %) and the Q-switch frequency (Qsf). The laser is focused on a target material optically while being monitored using the built-in concentric camera. In order to determine optimal laser power and Q-switch frequency for selectively etching the target material, an array of patterns (here, squares) is marked with varying parameters (Figure A4.2). Scan speed is kept constant at 150 mm/s. The laser marked regions are checked under the optical microscope to find the right conditions that avoids etching of underlying Si/SiO₂ (300 nm). Hyperspectral imaging can also be used to find the reflection contrast of the etched regions with respect to that of the substrate and therefore, appropriate marking conditions (Figure A4.2). We note that the conditions might vary depending on the fill pattern within the squares (cross, slant, linear) and when using a modified laser setup

for higher resolution patterning. Therefore, a power dependent assay is suggested before patterning any target material. The sample is placed on the sample stage and marked using the optimized conditions. A flow of nitrogen is introduced to remove any debris.

The as-bought laser marking setup which has a $100 \times 100 \text{ mm}^2$ field of view is used for the large-scale patterning. The line resolution in this case without modification is $\sim 10 \mu\text{m}$, limited by the numerical aperture (NA) of the in-built telecentric lens which is 0.021 (Figure A4.3 a, b, c). The setup is modified to increase the NA of the system to ~ 0.6 for sub- μm line resolution as shown in Figure A4.3d, e. It is modified based on the 4f-imaging technique or the Keplerian beam reducer design.⁹⁵ Therefore, the modular optics set-up enables compatibility between original large-scale patterning and sub-micrometer scale high resolution patterning ability (Figure 4.5).

Laser patterning to define channel based on TMDs. A 1 cm^2 shadow mask containing 500 by 500 μm^2 windows is placed onto monolayer TMD and the exposed areas are etched using the laser marker. 1 nm Ti/50 nm Au is e-beam evaporated onto the sample. These large metal pads are later used only for electrically probing the material. We note that the previous step of TMD etching is crucial to ensure stronger adhesion of pads to the substrate which otherwise might lead to their peeling off during actual electrode transfer. For the same reason, Ti adhesion layer is used. The channel width is now defined by patterning the TMD aligned with the large metal pads.

Non-perturbative electrode transfer.

Preparation of electrodes via photolithography. A bare Si/SiO₂ (300 nm) substrate is first cleaned with acetone, IPA and nitrogen blow dried. It is further cleaned with O₂ plasma for a minute followed by e-beam evaporation of 50 nm thick gold. We spincoat $\sim 4 \mu\text{m}$ thick AZ1518 resist on top of Si/SiO₂/Au and soft bake at 95 °C for 60 s. We note that this will act as a polymer spacer

during electrode transfer and avoid direct contact between PDMS and TMD in later steps. The AZ1518 can be replaced with other polymers such as SU8 with similar or higher thickness (~10-25 μm). Transfer electrode design (each pad should be smaller than the larger Au pads deposited earlier for probing, here $\sim 340 \times 400 \mu\text{m}^2$) is UV exposed and developed in AZ 300 MIF for 90 s. The bare Au after development is plasma etched using 4 sccm Cl_2 / 16 sccm Ar for 1 minute. Thus, Au/AZ1518 structures are defined on the substrate.

Transferring electrodes on pre-patterned TMD samples. In order to peel the Au/AZ1518 off of the substrate, the Au/AZ1518 pre-designed electrodes are exposed to water vapor for 10-30 seconds to reduce the adhesion between Au and Si/SiO₂. Soon after vapor exposure, PDMS is placed on top of the Au/AZ1518 template, lightly pressed and then placed on a transfer stage. We bring a PF Gel-film (Gel Pak - PF-40-X8) with a double-sided tape attached to it from the top and press it against the Au/AZ1518 template. We lift up the top PDMS/tape which then picks up the bottom Au/AZ1518/PDMS structure. We now place the pre-patterned TMD sample with defined channel width on the transfer stage. The picked-up Au/AZ1518/PDMS is pressed against the sample in an aligned manner. Once properly contacted, the temperature of the transfer stage is increased to 80°C and is held as such for 1-2 minutes. Finally, the PDMS is lifted off slowly from the sample to release the Au/AZ1518 (transfer stage still at 80 °C).

Figures

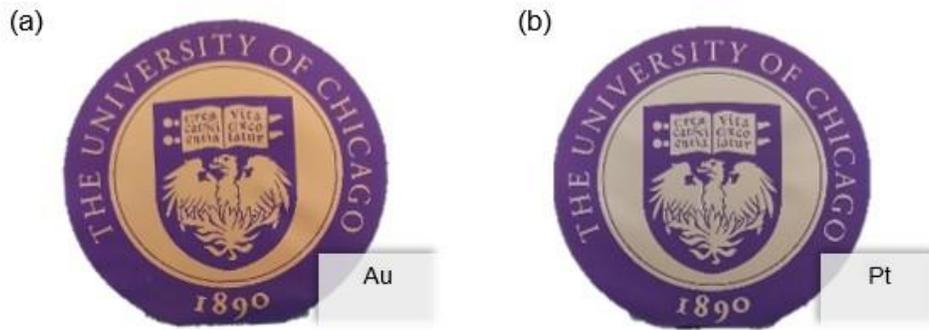


Figure A4.1 Laser patterning of metal films. (a, b) Photographs of laser-patterned thin-film materials deposited on 50 mm diameter Si/SiO₂ (300 nm) substrates: (a) Au (50 nm thick); and (b) Pt (50 nm thick).

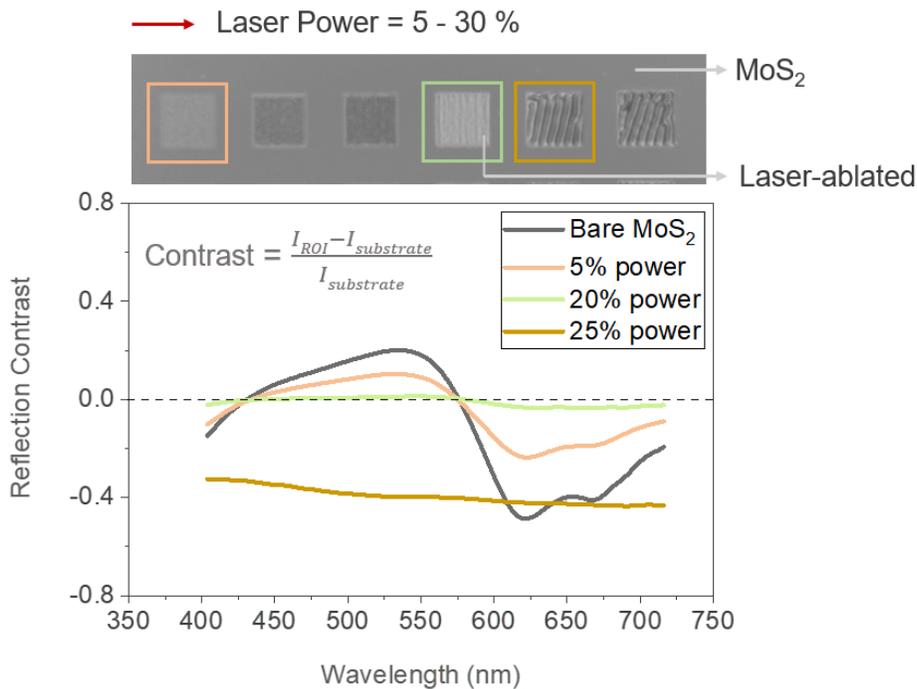


Figure A4.2 Optimization of laser patterning parameters for selective etching of MoS₂. Top: A reflection image at 600 nm wavelength showing square patterns (area of each square, 100 × 100 μm²) made upon etching monolayer MoS₂ on Si/SiO₂ (300 nm) substrate using laser powers varying from 5% to 30% (Q-switch frequency is kept constant at 400 kHz; laser scan speed at 150 mm/s). Bottom: Reflection contrast as a function of wavelengths for the three boxed laser ablated regions of interest (ROI) of top image. Reflection contrast is defined as (I_{ROI} – I_{substrate})/I_{substrate}, where I_{ROI} and I_{substrate} are the reflection intensities from ROI and from the bare Si/SiO₂ (300 nm) substrate respectively.

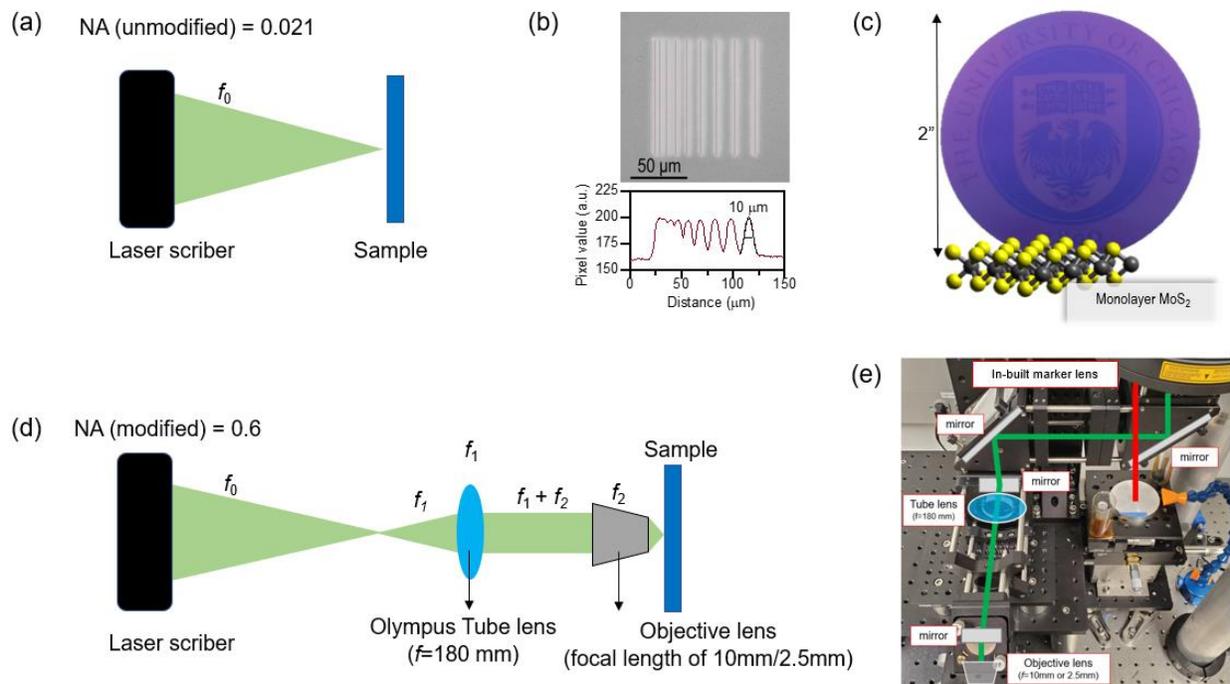


Figure A4.3 Flexibility in scale and resolution of patterning depending on the optical elements of laser marking setup. (a) Schematic of laser marking setup showing the laser scribe and the sample position for unmodified, as-bought setup. (b) Optical micrograph of laser-patterned MoS₂ (top) and corresponding extracted line profiles (bottom) for unmodified setup showing the line resolution to be $\sim 10 \mu\text{m}$. (c) Photograph of laser patterned monolayer MoS₂ on a 2-inch Si/SiO₂ wafer enabled by the unmodified laser marking setup. (d) Schematic of laser marking setup showing the laser scribe and the sample position for modified, image reducer setup for improved sub- μm resolution, which utilizes a tube lens and an objective lens with different focal lengths. (e) Photograph of the laser marker setup. The green and red lines show the beam paths for modified and unmodified setups respectively.

CHAPTER 5

MEASUREMENT OF ELECTRICAL CONDUCTIVITY FROM GROWTH TO DEVICES

5.1 Introduction

To achieve reliable and desirable performance of monolayer TMD based devices, a few characteristics for performing electrical measurements should ideally be met. A measurement approach with three features including non-perturbative patterning, non-perturbative transfer of contacts and batch production of devices was introduced in the last chapter. Here, we will show how we use this to probe the electrical properties of the starting material and understand the effects of individual device fabrication step on the material.

We will use the non-perturbative measurement approach as a tool to study the electrical properties of large-scale monolayer TMDs, including MoS₂ and WSe₂, and then systematically monitor the evolution of those properties along various stages of common electron-beam and photolithography processes, specifically for MoS₂ FETs. The monitoring of electrical properties starts from measuring the properties of as-grown, pristine films. This acts as a reference to probe the modifications to the electrical properties caused during the lithography processes. Our measurements reveal that simple exposure to solvents like acetone changes the electrical conductivity of MoS₂ much more than the rest of the processes, including the exposure to photo or electron-beam resists which have surprisingly negligible effects. We further conduct systematic measurements to show that exposure to different solvents leads to different on-state conductance of MoS₂, an effect that can be explained by a solvent-induced doping effect and their electronegativities. This chapter is largely adapted from Ref. 90.

5.2 Non-Perturbative Measurements of Electronic Properties of as-grown TMDs

Figure 5.1a plots the sheet conductivity (σ_{\square}) vs backgate voltage (V_{BG}) curves measured from an array of 20 MoS₂ channels with the same dimensions as shown in Figure 4.8b of Chapter 4. All the MoS₂ devices show similar behaviors. The measured σ_{\square} is very low ($< 10^{-5}\mu\text{S}$) for negative V_{BG} and increases for positive V_{BG} by approximately four orders of magnitude, reaching around $0.01\mu\text{S}$ at $V_{BG} = 80\text{V}$. The curves show an exponential V_{BG} -dependence near $V_{BG} = 0\text{V}$, which suggests that they are in the sub-threshold regime. For comparison, a $\sigma_{\square} - V_{BG}$ curve (dotted line) measured from a similarly grown MoS₂ film is shown, where the electrodes and channels are fabricated using conventional photolithography and direct deposition. It shows a much higher σ_{\square} (more than 100 times higher) and a linear V_{BG} -dependence, in contrast to the results of the non-perturbative measurements. σ_{\square} increases further after the deposition of a hafnium oxide dielectric on the surface (dashed line), and measurements from multiple such devices yield a high electron mobility ($21 \pm 4\text{ cm}^2/\text{V}\cdot\text{s}$). Figure 5.1b shows a similar comparison conducted using monolayer WSe₂. Using the non-perturbative measurement approach, the WSe₂ channels exhibit high σ_{\square} at negative V_{BG} that decreases with increasing V_{BG} . The mobility of as-grown WSe₂ channels is $8 \pm 3\text{ cm}^2/\text{V}\cdot\text{s}$. In contrast, electrical measurements carried out via a conventional photolithography-based approach show a drastically different response (dotted line), exhibiting much lower conductivity.

The data in Figure 5.1a and 5.1b clearly illustrate that significant differences occur in the measured conductivities of monolayer TMDs when different measurement approaches are used. It also explains how such comparisons can be used to monitor the properties of TMD starting from

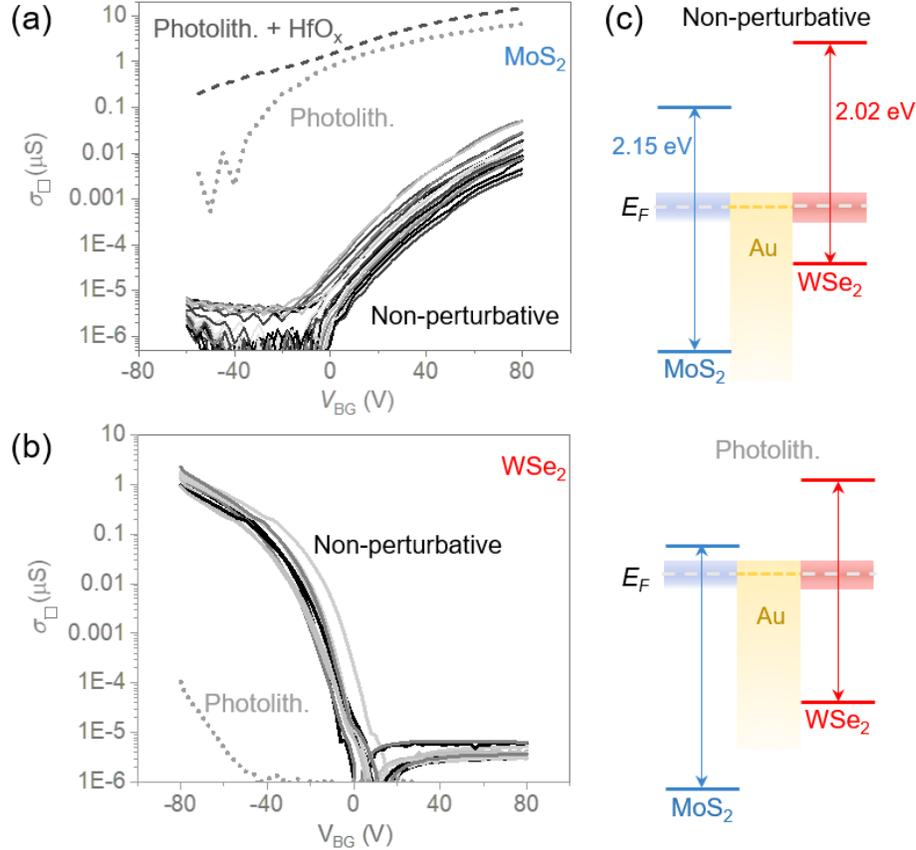


Figure 5.1 Non-perturbative electrical properties of as-grown TMDs. (a) and (b) Sheet conductivity vs back gate voltage for (d) MoS₂ and (e) WSe₂ channels respectively. Solid lines: non-perturbative measurement; Dotted lines: photolithography-based measurement; dashed line: measurement involving photolithography combined with hafnium oxide dielectric deposition. (c) Band alignments of MoS₂ (or WSe₂) and gold (work function ~ 5.1 eV)¹⁵ expected for non-perturbative measurement (top) and after photolithography (bottom). E_F is the Fermi level of the system. The energy levels are drawn considering free-particle band gaps of MoS₂ and WSe₂.²⁹

the growth and during a device fabrication process. First, our non-perturbative measurements probe their properties as grown, providing reference points. Our data in Figure 5.1a and 5.1b suggest that the MoS₂ channels exhibit lightly doped, *n*-type conductivities while the WSe₂ channels show a *p*-type behavior. This is consistent with the expected band alignments between MoS₂ (or WSe₂) and gold (see Figure 5.1c, top). The schematic band alignment is drawn considering the free-particle bandgaps of MoS₂ and WSe₂.²⁹ The concept of free-particle bandgaps has already been discussed in Chapter 2. Second, comparing these results with the lithography-

based measurement approach shows the net effect of the processes used for the device fabrication. In our experiment, the particular photolithography process leads to a further n -type doping of the TMD channels, increasing σ_{\square} of MoS₂, which is n -type as-grown, and decreasing σ_{\square} of WSe₂, which is p -type (see Figure 5.1c, bottom).

5.3 Evolution of MoS₂ Conductivity During Conventional Lithography Processing

The changes of σ_{\square} observed in Figure 5.1 after the photolithography are a result of the combined effects of many steps applied to the as-grown TMD monolayers. Our non-perturbative

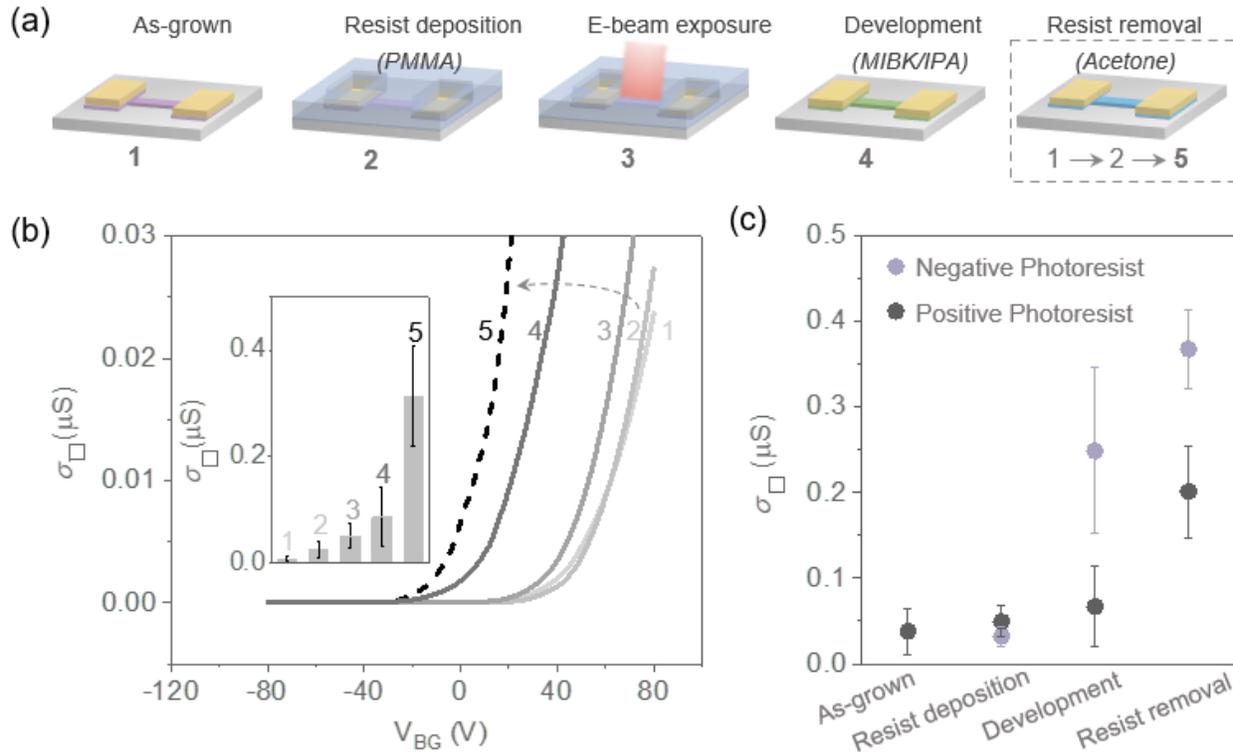


Figure 5.2 Effect of conventional lithography processes on MoS₂ conductivity. (a) Schematic of MoS₂ channels at different fabrication steps involved in EBL. (b) Representative transfer curves of as-grown MoS₂ and ones obtained at numerically-designated process steps in (a) of EBL. Inset: Mean on-state conductivity from 15 devices at each step. (c) Mean on-state conductivity (each from 11 devices) of MoS₂ channels during different processing steps of photolithography, plotted for two different photoresists.

measurements can be used to resolve the effect of individual fabrication steps, including, for example, resist coating, exposure, development, and resist removal. In Figure 5.2, we demonstrate this by measuring the changes in σ_{\square} after each step during an example electron beam lithography (EBL) process. Figure 5.2a shows a schematic of MoS₂ channels at various processing steps of EBL, whose conductivity is measured and compared to that of unprocessed, as-grown MoS₂ channel, measured non-perturbatively (1), which acts as a reference. The EBL process involves poly-methyl methacrylate (PMMA) resist deposition (2), e-beam exposure (3), and development in methyl isobutyl ketone in isopropanol (MIBK/IPA) (4). We measure the $\sigma_{\square} - V_{BG}$ curves after each step. In addition, we measure the effect of acetone-based removal of PMMA (1→2→5) without exposure to e-beam and a developer solution. Slightly different experimental procedures are used for each checkpoint to enable non-perturbative measurements as explained in the Appendix section.

Figure 5.2b shows representative $\sigma_{\square} - V_{BG}$ curves measured at these checkpoints. The curves shift progressively towards more negative gate voltages going from (1) to (5), where the magnitude of the shift, ΔV_{BG} (measured with respect to curve 1) varies for each step. ΔV_{BG} is small after the deposition of PMMA (2) and an e-beam exposure (3). There are considerable increases in ΔV_{BG} after the development (4) by ~ 40 V and after an acetone-based PMMA removal (5) by ~ 60 V. The inset in Figure 5.2b plots the average σ_{\square} measured at $V_{BG} = 80$ V (each based on results from 15 devices) and shows an increasing σ_{\square} from (1) to (5). The increase in σ_{\square} at a positive V_{BG} and the negative shift of the $\sigma_{\square} - V_{BG}$ curves, both suggest that each step during the EBL induces further *n*-type doping. In particular, our data suggests that the doping effects from the steps that involve the exposure to solvents (MIBK/IPA developer in (4) and acetone in (5)) are larger than those from other steps. Based on the ΔV_{BG} values in Figure 5.2b, we estimate the increase in the

carrier concentration (n_{2D}) in MoS₂ to be $\sim 3 \times 10^{12} \text{ cm}^{-2}$ after (4) and $\sim 4 \times 10^{12} \text{ cm}^{-2}$ after (5), using the parallel-plate capacitor model.¹³ In Figure 5.2c, we carry out a similar set of studies for a typical photolithography process using different resists (positive and negative). The mean σ_{\square} measured at $V_{BG} = 80 \text{ V}$ from multiple channels after different process steps are shown. The results are similar to the EBL results. σ_{\square} remains low after the resist deposition but it increases significantly, both, after development (using a water-based developer) and resist removal (using acetone). This leads to a surprising conclusion: an exposure to e-beam- or photoresists causes relatively small changes to σ_{\square} , whereas the steps that remove them using solvents (a developer or acetone) result in much larger changes. This is different from a widely cited cause for the process-induced doping in TMDs and graphene, which was thought to be due to the resists.^{76-80,96}

5.4 Effect of Solvents on MoS₂ Conductivity

The conclusion in Figure 5.2 also suggests that exposure to liquid solvents directly affects σ_{\square} of TMD channels, the degree of which may vary for each solvent. This is indeed what we observe in our experiments shown in Figure 5.3. We investigated the effects of commonly used organic solvents on σ_{\square} of MoS₂ using our non-perturbative measurement technique. For this, two MoS₂ samples are made and probed non-perturbatively; one is as-grown (to be used as a reference), and the other is immersed in a specific solvent overnight (see the schematic in Figure 5.3a). Figure 5.3b shows representative $\sigma_{\square} - V_{BG}$ curves measured after acetone, heptane, and chloroform exposure alongside a curve from as-grown MoS₂. The plot shows different effects from each of the three solvents. First, exposure to heptane does not significantly change σ_{\square} of MoS₂, in contrast

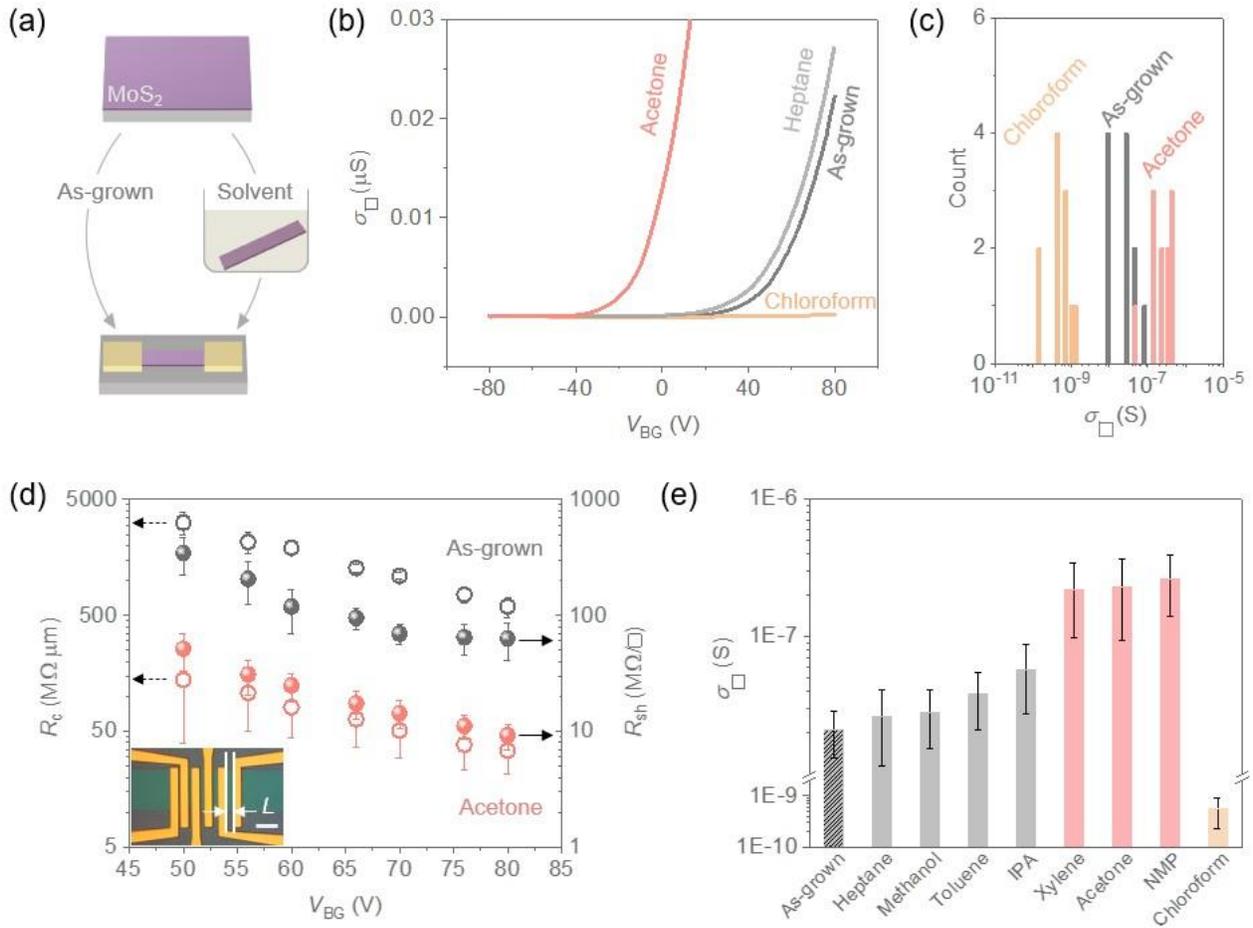


Figure 5.3 Effect of organic solvents on MoS₂ conductivity. (a) Schematic of experimental pathway to study the solvent effects. (b) Representative transfer curves of as-grown MoS₂ and ones obtained after exposure of channels to acetone, chloroform and heptane. (c) Histograms of on-state conductivities at $V_{BG} = 80$ V corresponding to the channels shown in (b). (d) Contact and sheet resistance for as-grown and acetone-exposed MoS₂ measured using the transfer length technique. Inset: Optical micrograph of a device used for channel length measurements, where channel length, L is denoted. Scale bar is $50 \mu\text{m}$. (e) Mean on-state conductivities (each from 11 devices) for MoS₂ channels as-grown and treated with different organic solvents.

to the other two. Second, while acetone shifts the $\sigma_{\square} - V_{BG}$ curve in the negative V_{BG} direction ($\Delta V_{BG} \sim 70\text{V}$) significantly increasing σ_{\square} at $V_{BG} = 80$ V, the MoS₂ does not show any measurable conductance after being exposed to chloroform. This behavior is consistently observed from many devices, as shown in the histogram in Figure 5.3c. Overall, these data suggest that acetone induces further n -type doping of MoS₂, while chloroform has an opposite effect. This effect remains after

thermal annealing at up to 200°C (see Figure A5.1 of Appendix). It is noted that the acetone treatment does not change the surface morphology of MoS₂ as evident by the atomic force microscopy measurements (Figure A5.2). These imply that the doping effect is likely due to the chemical adsorption of solvent molecules on MoS₂ surface, not because of physical adsorption. The additional *n*-doping after acetone exposure also results in the increase in the overall conductivity as well as the lowering of the contact resistance. We further extract the values of the contact (R_c) and sheet resistance (R_{sh}) of MoS₂ channels (as grown vs after acetone exposure) using non-perturbative measurements based on the transfer length technique⁹⁷⁻¹⁰⁰ as shown in Figure 5.3d. R_c and R_{sh} both become lower after acetone exposure by 1~2 orders of magnitude compared to those of the as-grown channels. In particular, the lower R_c of acetone-exposed MoS₂ is consistent with the *n*-doping effect of acetone, as it lowers the width of the Schottky barrier at the contact. The concept of narrowing of the depletion width upon increased doping has been discussed in Chapter 3. The result, therefore, suggests that direct exposure to various solvents could be useful for systematically tuning the electrical properties of TMDs.

Figure 5.3e compares σ_{\square} of MoS₂ at $V_{BG} = 80$ V (each averaged from 11 devices) after exposure to 8 different organic solvents. There are roughly three categories of behaviors. The first set comprises heptane, toluene, methanol and isopropyl alcohol, all of which cause minimal change to the MoS₂ conductivity. The second set of solvents (xylene, acetone and *n*-methyl-2-pyrrolidone (NMP)) increases the conductivity by roughly an order of magnitude. The final one is chloroform which lowers the conductivity. One parameter that may explain the different doping effect by a solvent is its electronegativity (χ) as previously cited;⁸⁹ a difference in χ generally leads to charge transfer from the system with lower χ to the one with higher χ . Comparing the available values of χ for MoS₂ (~ 5.1 eV) and several solvents (see Table A5.1 of Appendix) suggests that solvents

with a smaller χ lead to further n -doping (acetone ~ 4.1 eV, xylene ~ 3.6 eV), chloroform with a higher χ (~ 5.5 eV) leads to the opposite effect, and heptane with χ (~ 5 eV) similar to MoS₂ causes little change. However, this correlation is not universal; for example, toluene with $\chi \sim 3.8$ eV does not lead to n -doping. Indeed, the interactions between monolayer films and solvent molecules are complex and influenced by other factors (*e.g.*, charge rearrangement, molecular orientation, etc.) as discussed in other studies.^{101,102} Our non-perturbative measurements could thus provide precise information, separate from the effects of lithography and allow the careful study of such molecule-TMD interactions in the future.

5.5 Summary

In this chapter we have demonstrated the utility of the non-perturbative measurement method enabled by direct laser patterning and electrode transfer. We used this approach to monitor the electrical properties of monolayer TMDs from growth to devices. Our experiments successfully resolve the effects from individual steps of conventional lithography processes and find that common solvents introduce different doping effects. The solvent doping can serve as a knob to systematically tune the electrical properties of TMD based devices. Moreover, our non-perturbative technique offers a much-needed platform that can be applicable to various surface-sensitive materials during the testing and development of processes for controlling their electrical properties.

5.6 Appendix

Methods

Probing effects of processing steps during conventional lithography.

For E-beam Lithography. PMMA deposition. In order to study effect of PMMA deposition statistically, we refrain from making non-perturbative devices and spincoating PMMA as this tends

to damage the transferred electrodes and affects the yield. Instead, we directly transfer the PMMA coated gold transferred electrodes. Therefore, we first prepare the 50 nm thick gold electrodes on bare Si/SiO₂ substrate via conventional photolithography. This is followed by spincoating 950K PMMA A4 onto it. We open parts of the PMMA film that upon alignment with larger gold pads of MoS₂ sample would later allow us to probe the TMDs, by e-beam exposure and development. We treat it with water vapor for a min and nitrogen blow dry. We then put a thermal release tape (TRT) on top of it and treat with vapor for 1 min to reduce the adhesion between PMMA and the substrate. The Au/PMMA/TRT template is gently peeled off. This is transferred in an aligned way onto MoS₂ sample (with large metal pads and channel width already defined) on a transfer stage at room temperature. The TRT is released at 140 °C. At this stage, the channel area is PMMA encapsulated and we have bare Au areas for probing. E- beam exposure. The MoS₂ channel regions of above PMMA encapsulated samples alone are exposed to the e-beam (Raith EBPG 5000 Plus E- beam writer – 25 nA current, dose of 1200 $\mu\text{C}/\text{cm}^2$, 300 μm aperture size, 100 kV accelerating voltage). Development. We start by spincoating 950K PMMA A4 and baking at 160 °C for 90 s onto the as-grown MoS₂ sample. We then expose the whole sample area with e-beam and develop the PMMA in MIBK: IPA (1:3) developer for 60 s. We then make the non-perturbative devices as described above. PMMA removal. PMMA is spun coat on MoS₂ and baked at 160 °C for 90 s. The PMMA is removed in acetone solvent overnight. The non-perturbative devices are then completed as described in Appendix of previous chapter.

For Photolithography. Resist deposition. Effect of resist deposition is studied similar to e-beam lithography process, except that the resists used are AZ1512 and AZ nLof 2020 positive and negative photoresists respectively. The pre-fabricated electrodes with open parts of the AZ1512 resist on top are treated to vapor for 30 s and a PDMS is put on top. Using Gel film/double sided

tape, the stack is picked and transferred on MoS₂ at room temperature. For AZ nLof 2020, PDMS treated with vapor for 10 s is placed on top of Au with partially opened nLof 2020 resist film. It is placed on a transfer stage set at 80 °C and using Gel film/double sided tape, picked up from the substrate and transferred on MoS₂. After few minutes, PDMS is lifted up to release the electrodes.

Development. MoS₂ with spin coated AZ1512 is exposed to 375 nm UV light and developed in AZ 300 MIF developer while for AZ nLof 2020 resist, the sample is directly developed in AZ 300 MIF without UV exposure. After development, non-perturbative devices are completed as described above. Photoresist removal. MoS₂ with spin coated AZ1512 is directly removed in acetone while for AZ nLof 2020 resist, the sample is exposed to UV light, post-exposure baked and then removed in acetone for few hours. After resist removal, the non-perturbative devices are then completed as described in Appendix of previous chapter.

Probing effects of organic solvents. In order to study the effect of solvents on MoS₂ conductivity, the as-grown MoS₂ samples are immersed in different solvents overnight. The samples are taken out of the solvents and nitrogen blow dried without any further rinsing. Finally, non-perturbative devices are fabricated.

Device fabrication using conventional photolithography. We start by spincoating resist bilayer on as-grown TMD sample; 495K PMMA A6 on the bottom and AZ 1512 positive resist on top. The pattern for defining the channel is UV exposed. The AZ 1512 is developed in AZ MIF 300 developer. It is rinsed with DI water and N₂ blow dried. Using O₂ plasma stripper, we remove the underneath PMMA layer. The TMD is etched using SF₆/O₂ plasma etching. The O₂ plasma strip step is repeated to get rid of any residual polymer. The remaining polymer is removed in acetone for few hours. In order to define source and drain electrodes, we use AZ nLof 2020 resist and UV expose it. We post-exposure bake and develop the polymer in AZ 300 MIF developer, rinse it in

DI water and N₂ blow dry it. We make sure that this step is carried out gently to avoid any delamination of MoS₂. This is followed by e-beam evaporation of 50 nm Au which is then lifted off in acetone overnight.

Electrical measurements. All electrical measurements were done under ambient conditions in a two-probe geometry, using an Agilent B1500 Device Analyzer except for MoS₂ photolithography devices which were measured using a home-built probe station.

Figures

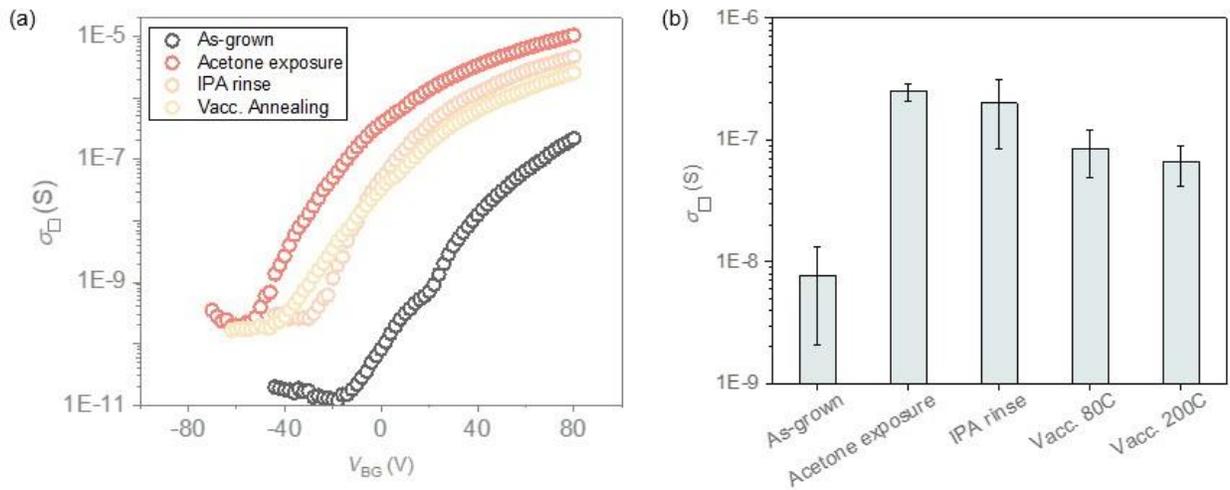


Figure A5.1 Effect of thermal annealing on MoS₂ conductivity after acetone exposure. (a) Representative sheet conductivity vs back gate voltage curves obtained for as-grown MoS₂, MoS₂ after acetone exposure, IPA rinse following acetone exposure of MoS₂ and vacuum annealing (at 80°C) following acetone exposure of MoS₂. (b) Mean on-state conductivity (each from 11 devices) of MoS₂ channels corresponding to the processing steps shown in (a); vacuum annealing at 80°C and 200°C.

The data suggests that even after subsequent processing the induced *n*-doping effect after exposure to acetone is retained and not entirely reversed.

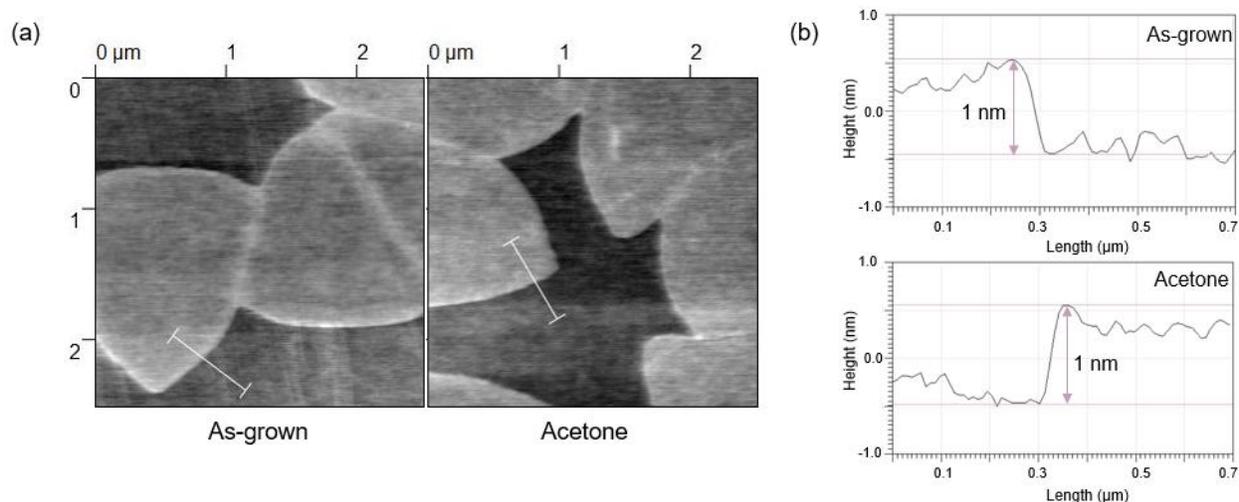


Figure A5.2 Atomic Force Microscopy of MoS₂ before and after acetone treatment. (a) Atomic force microscopy images of as-grown MoS₂ surface (left) and after acetone exposure (right). (b) Cross sectional height profiles obtained along the lines in the images shown in (a). Top is for the as-grown MoS₂ surface and bottom, for an acetone treated surface.

Table

Electronegativity values of solvents: The electronegativity (χ) of a molecule is given by $(IP + EA)/2$, where IP is the ionization potential and EA is the electron affinity.^{89,103} Therefore, the electronegativity values of solvents whose IP and EA values could be obtained have been tabulated in Table A5.1.

Solvents	IP^{104}	EA	χ
Chloroform	11.4 eV	-0.35 eV ¹⁰⁵	5.5 eV
Toluene	8.8 eV	-1.1 eV ¹⁰⁶	3.8 eV
<i>p</i> -Xylene	8.4 eV	-1.07 eV ¹⁰⁶	3.6 eV
Acetone	9.7 eV	-1.51 eV ¹⁰⁶	4.1 eV
Heptane	9.9 eV	0.2 eV ¹⁰⁷	5.0 eV

Table A5.1. Ionization potentials, electron affinities and electronegativity values of solvents.

Electronegativity value of MoS₂: The electronegativity of MoS₂ is calculated from the equation – $\chi (\text{MoS}_2) = E_{\text{VBM}} + E_e - E_g/2$, where E_{VBM} is the valence band maxima or edge potential with respect to standard hydrogen electrode, E_e is the energy of free electrons on the hydrogen scale (4.5 eV), E_g is the band gap.^{89,108,109} Taking values of E_{VBM} and E_g for MoS₂,²⁶ we calculate $\chi (\text{MoS}_2) \sim 5.1$ eV.

CHAPTER 6

CONTROLLED TUNING OF ELECTRICAL CONDUCTANCE VIA SUBSTITUTIONAL DOPING

6.1 Introduction

In the previous two chapters, we demonstrated the near-ideal electrical measurement approach for surface-sensitive atomically thin semiconductors and used it to study their pristine properties which can serve as a baseline to probe the effects of any subsequent processing step and chemical exposure. This provides a perfect platform for probing and tuning of electronic properties. As discussed in Chapter 3, substitutional doping during the material synthesis is an effective way to dope the TMD films and tune their electronic properties. Existing efforts^{53,54,110} based on CVD have demonstrated the feasibility of direct substitution of Mo with Nb or Re in 2D monolayer MoS₂. However, in all these studies conventional lithography-based device fabrication/measurement approaches were used and they can significantly impact the transport properties of TMD FETs. Due to the interference of contributions from the substitutional dopants and the measurement approach, it is difficult to accurately identify the net effect of the intentionally introduced dopants. Besides, the variable control of the dopant concentration over a large scale is currently lacking.

In this chapter, which is mainly adapted from the Ref. 111 (Hui Gao *et al.* Nano Letters 2020), to which I am a co-author, we will address this challenge. To do this, we do large-scale growth of monolayer MoS₂ that can directly incorporate Nb and Re into the films and employ the laser-based fabrication method to avoid any unwanted doping from the conventional lithography process. Our electrical data successfully reveal the impact of the substitutional dopants alone, which is necessary to confirm the tunability of the conductance via modulation of the doping

concentration. Our results further allow a systematic understanding of the conduction mechanism in the 2D limit. Finally, we demonstrate the stability of the dopants and the potential application of the doped MoS₂ through the fabrication of lateral junctions.

6.2 Precise Control of Dopant Concentration During Growth

Figure 6.1 presents wafer-scale, continuous MoS₂ monolayers grown with substitutional dopants. As a representative example, Figure 6.1b shows optical images of the MoS₂ films substitutionally doped with Nb (left; Nb-MoS₂) and Re (right; Re-MoS₂), both grown on 1-inch fused silica substrates. An intrinsic, with no dopants, MoS₂ monolayer (middle; *i*-MoS₂) is included for comparison. Both Nb-MoS₂ and Re-MoS₂ appear uniform over the entire area of the wafer, similar to the *i*-MoS₂. The color of the doped materials can be seen to vary slightly from the *i*-MoS₂ with the introduction of Nb or Re. Figure 1c presents an atomic-resolution scanning transmission electron microscopy (STEM) image taken from a Re-MoS₂ sample grown with Re dopant concentration, $C_{\text{Re}} = 10\%$. It shows the hexagonal crystalline lattice of MoS₂, where some Mo sites are brighter than the rest of the atoms in the lattice. These brighter spots correspond to

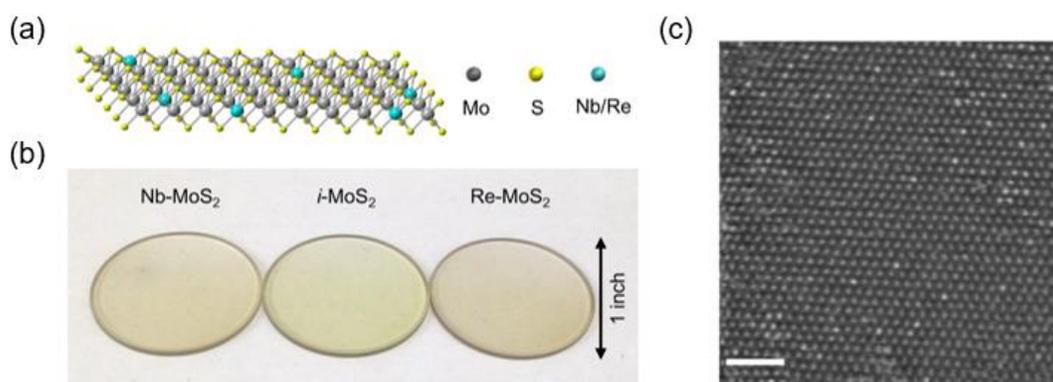


Figure 6.1 Large-scale Nb- and Re-doped monolayer MoS₂. (a) Ball & stick model for the substitutional doping of MoS₂ using Nb and Re. (b) Optical micrograph of intrinsic and doped MoS₂ monolayers grown on 1-inch fused silica. (c) STEM image of Re-MoS₂. Brighter atoms are Re and the darker atoms are Mo. Scale bar: 2 nm.

Re atoms, which have a higher atomic number than Mo. Notably, the Re atoms are distributed randomly through the lattice of MoS₂ without aggregation. This confirms the presence and substitutional incorporation of Re in the MoS₂ lattice.

Our doped MoS₂ monolayers were grown using a metal-organic chemical vapor deposition (MOCVD) process (See schematic in Figure 6.2a) specifically designed to achieve tunability and wafer-scale homogeneity. The MOCVD reactor used in our experiment is based on the one developed previously¹⁸ for the wafer-scale synthesis of undoped monolayer TMDs (*e.g.*, MoS₂, WS₂, WSe₂). The doping was carried out, by introducing the dopants in small quantities throughout

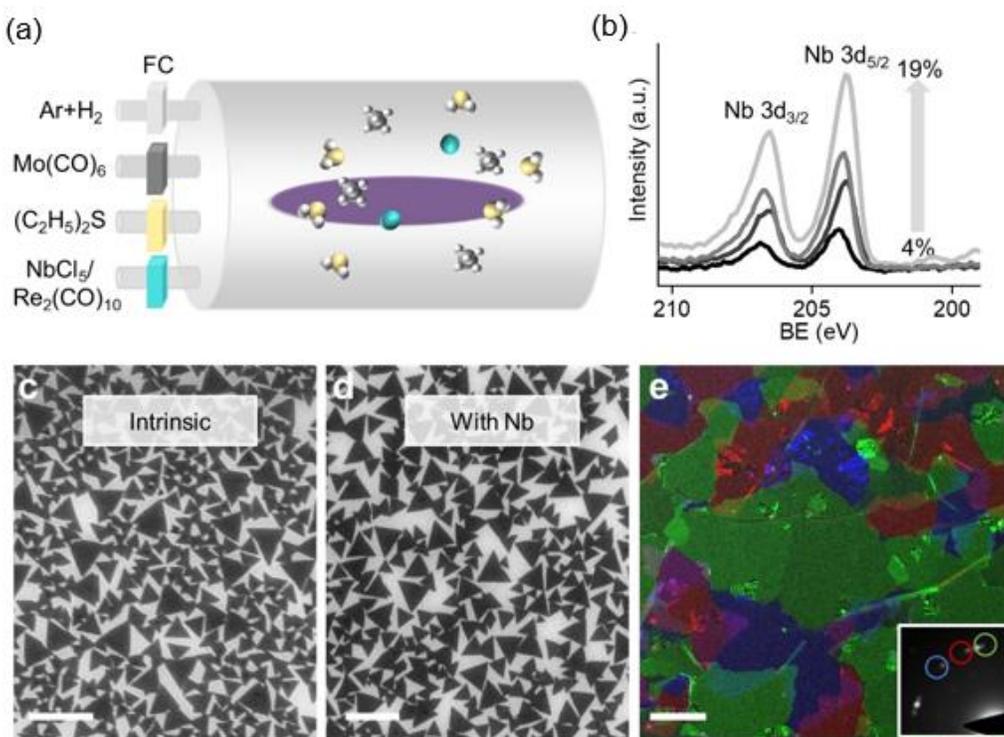


Figure 6.2 MOCVD growth of doped MoS₂. (a) Schematic of the MOCVD system for the growth of doped MoS₂ using all gas-phase precursors. Metering valves are used as the flow controllers (FC) for the Nb and Re precursors, while mass flow controllers (MFCs) are used for the other precursors and carrier gases. (b) XPS spectra showing doping concentrations for different Nb-MoS₂ films. From bottom to top: $C_{\text{Nb}} = 4\%$, 8% , 11% and 19% . (c) and (d) Representative SEM images of *i*-MoS₂ and Nb-MoS₂ ($C_{\text{Nb}} = 10\%$) grown for partial coverage, respectively. The scale bars are 200 nm. (e) False-color DF-TEM image of Nb-MoS₂ ($C_{\text{Nb}} = 10\%$) with the corresponding diffraction pattern shown in the inset. Scale bar: 200 nm.

the growth of the MoS₂. In order to control the amount of Nb and Re, NbCl₅ and Re₂(CO)₁₀ were used as precursors that were introduced into the reactor in the gas phase. The flow rates were precisely regulated using Ar carrier gas and careful temperature control. In this manner, we have identified optimized growth parameters for the synthesis of MoS₂ monolayers that are continuous over the entire substrate, where the concentration of Nb or Re in the MoS₂ lattice is reproducibly tuned over a wide range up to 20%. While we refer to these monolayers as doped MoS₂ in this report, they can also be considered as 2D alloys in the upper limit of the tuning range (20%).

The direct tuning of dopant concentrations in MoS₂ monolayers is confirmed by X-ray photoelectron spectroscopy (XPS), which is used to quantitatively measure C_{Nb} or C_{Re} . For example, the XPS data measured from four Nb-MoS₂ monolayers with different C_{Nb} are shown in Figure 6.2b. All four spectra clearly show peaks in the Nb 3d region (204 eV and 207 eV) corresponding to the Nb-S bonds that are absent in the *i*-MoS₂. The integrated area of the Nb peaks, normalized to the area of the Mo 3d peaks, provides a direct measure of C_{Nb} , as shown in Figure 6.2b. The measured C_{Nb} monotonically increases with the flow rate of NbCl₅, with a direct and reproducible correlation between the two. For the Re-MoS₂ sample shown in Figure 6.1c, we find that the value of C_{Re} measured using XPS (10%) is similar to the concentration of Re spots estimated from the STEM data (9%).

The doped MoS₂ monolayers display a spatially uniform dopant distribution as well as polycrystalline structure similar to that of *i*-MoS₂. Figures 6.2c and 6.2d present Scanning Electron Microscopy (SEM) images of two MoS₂ samples (*i*-MoS₂ and Nb-MoS₂ where $C_{\text{Nb}} = 10\%$), each grown under the same conditions (temperature, time, etc.) except for the introduction of Nb during the growth of the sample in Figure 6.2d. Both samples show triangular crystallites with similar growth rates, grain sizes, and nucleation densities. Increasing the growth time produces a

polycrystalline monolayer of doped MoS₂ with full coverage over the entire substrate. A false-color dark-field transmission electron microscopy (DF-TEM) image of such a continuous Nb-MoS₂ sample is shown in Figure 6.2e. In addition, the dopant concentrations (based on XPS data), measured after stopping the growth at different times, remains constant (*i.e.*, the concentrations are the same whether the film is partial or continuous). This implies that the incorporation of the dopants takes place uniformly throughout the growth. Altogether, the data in Figure 6.1 and 6.2 show that we have grown wafer-scale, continuous MoS₂ monolayers with a tunable concentration of substitutional dopants.

6.3 Tunable Electrical Conductivity of MoS₂ Upon Nb Doping

We now move to study the electrical conductance (σ_S , sheet conductance) of these doped films as a function of the dopant concentration, focusing on Nb. To exclude the effects from unintentional doping during the lithography process, the devices were fabricated without any exposure of the MoS₂ to chemicals. Instead, a shadow mask is utilized to deposit metal electrodes (50 nm thickness of Au film) and scanning laser ablation (as discussed in Chapter 4) to define the MoS₂ channels ($200 \times 200 \mu\text{m}$). A representative device is shown in the inset of Figure 6.3a.

Figure 6.3 presents the electrical properties of Nb-MoS₂ with different C_{Nb} . The data was taken at ambient conditions. First, it can be seen that the as-fabricated *i*-MoS₂ monolayer devices ($C_{\text{Nb}} = 0\%$) do not show notable electrical conduction (see Figure 6.3a, back gate bias $V_{\text{BG}} = 0 \text{ V}$) with a measured sheet conductance, σ_S , below $10^{-5} \mu\text{S}/\square$. This is consistent with the properties of an intrinsic semiconductor and the results shown in Figure 4.8c. While the *i*-MoS₂ devices remain non-conductive within our V_{BG} range as fabricated, with Nb doping, the devices exhibit much higher conductance ($\sigma_S > 10^{-2} \mu\text{S}/\square$ for $C_{\text{Nb}} = 4\%$; Figure 6.3a). A second observation is that the σ_S

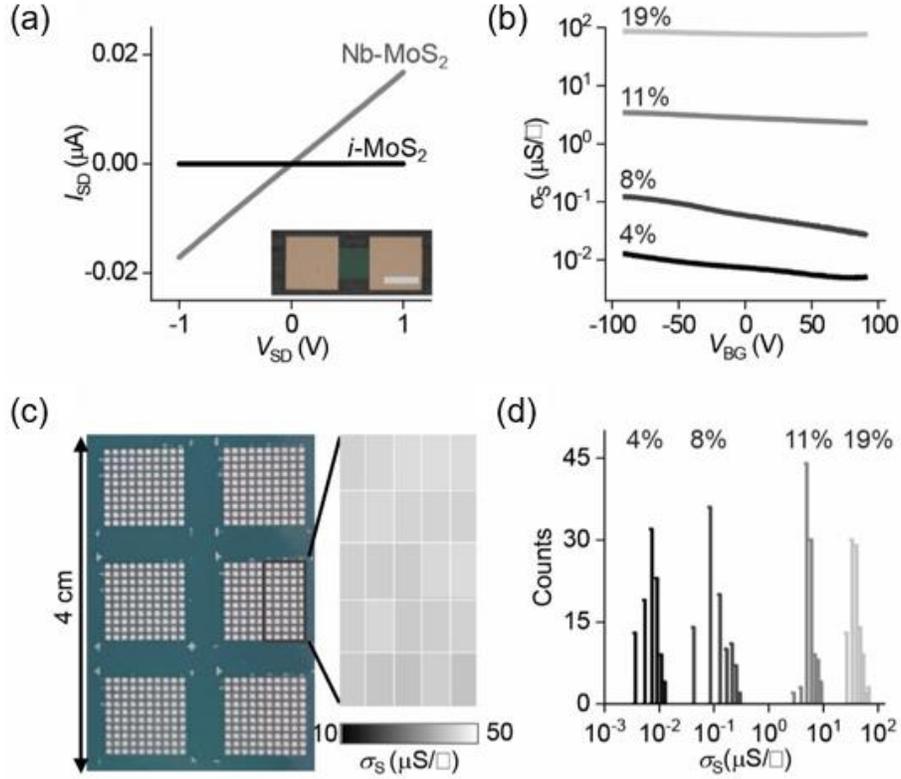


Figure 6.3 Tunable electrical conductance of doped MoS₂. (a) I - V curves of representative $i\text{-MoS}_2$ and Nb-MoS₂ ($C_{\text{Nb}} = 4\%$) devices measured at $V_{\text{BG}} = 0$ V. Inset: optical micrograph of a representative FET device. Scale bar: 200 μm . (b) Transfer curves of Nb-MoS₂ devices at different C_{Nb} . (c) Optical micrograph of a representative large-scale device array and the corresponding sheet conductance map for 25 devices. (d) Histograms of sheet conductance from four sets of 100 Nb-MoS₂ devices, each at different C_{Nb} .

of Nb-MoS₂ increases significantly with a higher Nb concentration. Figure 6.3b plots the gate transfer curves of four representative Nb-MoS₂ devices with C_{Nb} ranging from 4% to 19%. The highest σ_S is close to $10^2 \mu\text{S}/\square$ for $C_{\text{Nb}} = 19\%$, more than 7 orders of magnitude higher than that of $i\text{-MoS}_2$. The devices all show a p -type V_{BG} dependence. We note that the choice of the metal electrodes (Au vs. Pd) or the exclusion of contact resistance (2-probe vs. 4-probe measurements) have negligible effects on the measured σ_S of the Nb-MoS₂ devices in this doping concentration range. Finally, these electrical properties appear uniform over a large area. For example, the Nb-MoS₂ device array ($C_{\text{Nb}} = 19\%$) in Figure 6.3c exhibits a 100% device yield with a narrow

distribution of σ_S , as supported by the spatial map of σ_S (Figure 6.3c, right). Similar uniformity in σ_S is seen from device arrays fabricated for all values of C_{Nb} , four of which are plotted as histograms in Figure 6.3d. Each histogram, measured from 100 Nb-MoS₂ devices, shows a typical variation in σ_S of 30% relative to the mean. Our data in Figure 6.3 hence confirms the central experimental conclusion of this experiment that the electrical conductivity of a MoS₂ monolayer can be directly tuned by controlling C_{Nb} with large-scale spatial uniformity.

6.4 Localized dopants at the 2D limit

Our electrical data provide additional insight into the conduction mechanism in doped MoS₂ monolayers. Figure 6.4a plots the average σ_S as a function of C_{Nb} (solid circles, based on the data in Figure 6.3d.) alongside the 2D conductance ($\sigma = en\mu$, dotted lines) calculated for modest carrier mobilities under full ionization ($\mu = 1$ and $10 \text{ cm}^2/\text{Vs}$; $n = C_{Nb}/A/100$, where $A = \text{MoS}_2$ unit cell area) and previously reported data from electrostatically gated MoS₂^{18,99} (open circles, maximum carrier density corresponding to 0.5%⁹⁹ and 1.0%¹⁸ doping). Two observations can be made from this plot. First, σ_S of Nb-MoS₂ is significantly smaller than the calculated values and previous results, particularly at lower C_{Nb} . For example, our data at $C_{Nb} = 4\%$ ($\sigma_S < 10^{-2} \mu\text{S}/\square$) is at least two to three orders of magnitude lower than the calculated 2D conductance ($> 1 \mu\text{S}/\square$) and at least 1000 times smaller than the results from the electrostatically gated devices ($> 10 \mu\text{S}/\square$). Second, σ_S rapidly increases with C_{Nb} , with a nonlinear relationship between the two. σ_S changes exponentially with C_{Nb} , increasing its value roughly by an order of magnitude for every 4% increase in C_{Nb} . These observations indicate that the electrical conduction and tuning in substitutionally doped Nb-MoS₂ monolayers do not follow the conventional model based on fully ionized dopant carriers.

Previous theoretical reports^{112,113} have shown that substitutional dopants in monolayer MoS₂ have higher ionization energies (E_I) than in 3D MoS₂. For example, Noh, *et al.*¹¹³ predicted $E_I \sim 0.4$ eV for Nb or Re in monolayer MoS₂ on SiO₂, which is much larger than the thermal energy at room temperature ($kT \sim 26$ meV) or E_I in 3D MoS₂.^{114,115} This is primarily due to the weak screening of the Coulomb interaction in 2D materials, resulting in a dielectric constant ϵ (~ 3)¹¹⁶ in monolayer MoS₂, which is much smaller than the bulk value (~ 11).¹¹⁷ According to the hydrogen model, this smaller ϵ leads to a higher E_I for a dopant carrier (increasing as $1/\epsilon^2$) and a smaller Bohr radius (decreasing with ϵ) in monolayer MoS₂ (see illustration in Figure 6.4a, inset).

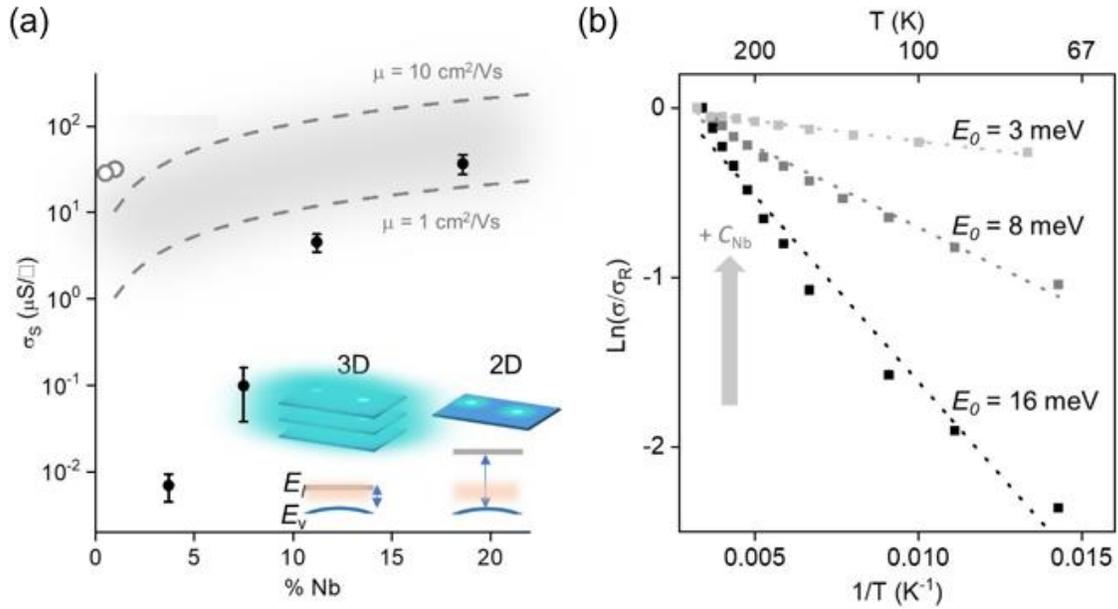


Figure 6.4 Localized dopants at 2D limit. (a) Semi-log plot of average σ_S (solid circles) versus C_{Nb} . The dash lines represent the expected σ_S assuming full ionization, with mobilities taken to be 10 and 1 cm^2/Vs for upper and lower dash lines, respectively. σ_S of electrostatically gated devices from references 18 (open circle, right) and reference 99 (open circle, left) are also included. Inset: band diagram showing the higher activation energy for dopant carriers in 2D materials that cannot be thermally activated at room temperature (kT shown in light orange). The glow around the cyan circle indicates the a_0 . E_v represents the valence band and E_I represents the dopant energy level. (b) Arrhenius plot of devices with $C_{\text{Nb}} = 8\%$, 11% and 19% (from bottom to top respectively). The best fit line for each data set, shown in the plot, is used to extract E_0 . The electrical conductance at various temperature is normalized to the room temperature conductance (σ_R).

Such a large E_I suggests an inefficient thermal ionization of dopant carriers in our Nb-MoS₂, similar to doped Si at low temperatures (or with deep dopant levels). The electrical transport in this $E_I \gg kT$ regime has been successfully described using the impurity conduction model,^{118,119} where the electrical conduction occurs through thermally activated hopping between localized dopant sites. The conductivity in this model is given by $\sigma = \sigma_0 \exp(-2R/a_0 - E_0/kT)$, where σ_0 is a prefactor independent of temperature and impurity density, a_0 is the Bohr radius of the dopant state, R is the average distance between dopants (dependent on dopant concentration), and E_0 is the hopping energy between the doping sites (typically an order-of-magnitude smaller than E_I). This model explains the main observations in Figure 6.4a. First, a larger C_{Nb} corresponds to a smaller R , which should lead to an exponential increase in σ and a significantly suppressed σ at a smaller C_{Nb} . Second, the electrical transport is thermally activated, as shown in Figure 6.4b. The estimated activation energy (E_0) ranges between 3 to 16 meV, much smaller than the predicted E_I . Finally, by fitting the experimental data in Figure 6.4a using the impurity band model, we quantitatively estimated $a_0 = 0.2$ nm, which is close to the value calculated based on a hydrogen model¹²⁰ with $\epsilon = 3$ and hole effective mass of $0.4 m_e$ for monolayer MoS₂, where m_e is the electron mass.

Together, the systematic investigation and tuning of the electrical properties of substitutionally doped MoS₂ suggest its potential application as a 2D conductor with tunable conductivity. In particular, Nb-MoS₂ with large C_{Nb} (e.g., 19%) shows a weak gate dependence (Figure 6.3b), a high σ_S (as large as 0.1 mS/□), and a measured Hall mobility close to 1.5 cm²/Vs that changes only slightly at low temperatures, indicating degenerately doped impurity band formation.

6.5 Doped MoS₂ as Stable Metallic Contacts

The doped 2D films with tunable, metal-like conduction can be used for producing atomically thin electrodes. Figure 6.5 shows the formation of a lateral edge contact between Nb-MoS₂ and *i*-MoS₂ that confirms the stability of the Nb-MoS₂ during the integration processes. For this, lateral junctions consisting of Nb-MoS₂ and *i*-MoS₂ are generated using a patterned regrowth method (schematic shown in Figure 6.5a). A Nb-MoS₂ monolayer is first grown on a SiO₂ substrate, then the film is patterned by conventional photolithography and reactive ion etching, after which *i*-MoS₂ is grown in the etched areas. Figure 6.5b shows an image of a representative Nb-MoS₂/*i*-MoS₂ heterostructure generated based on XPS mapping of the Nb 3d region. The brighter areas, corresponding to Nb-MoS₂ ($C_{\text{Nb}} = 11\%$), confirm the stability of the dopants throughout the chemical treatments involved in photolithography and the subsequent *i*-MoS₂ growth step that occurs at elevated temperatures (750 °C).

Figures 6.5c and 6.5d further present the electrical properties of a representative heterojunction device coated with 30 nm HfO₂ (see Figure 6.5c, inset). The Nb-MoS₂ channel (1-2, Figure 6.5c) exhibits a high $\sigma_S > 5 \mu\text{S}/\square$ with weak gate dependence, while the regrown *i*-MoS₂ channel (3-4, Figure 6.5c), after HfO₂ deposition, shows a characteristic *n*-type conduction with its conductance able to be switched on/off with gate bias. The electrical behavior confirms that the Nb dopants are stable during post-synthetic processing. Figure 6.5d shows the I - V curves measured from the region including the heterojunction (2-3) at different V_{BG} 's, suggesting a successful electrical connection across the junction with the overall properties largely determined by the properties of the individual parts. For example, when $V_{\text{BG}} = 0$ or -90 V, the current is limited by

the V_{BG} -dependent conductance of the i -MoS₂, whereas at $V_{BG} = 90$ V, the current is limited by the Nb-MoS₂, since i -MoS₂ is more conductive at that bias.

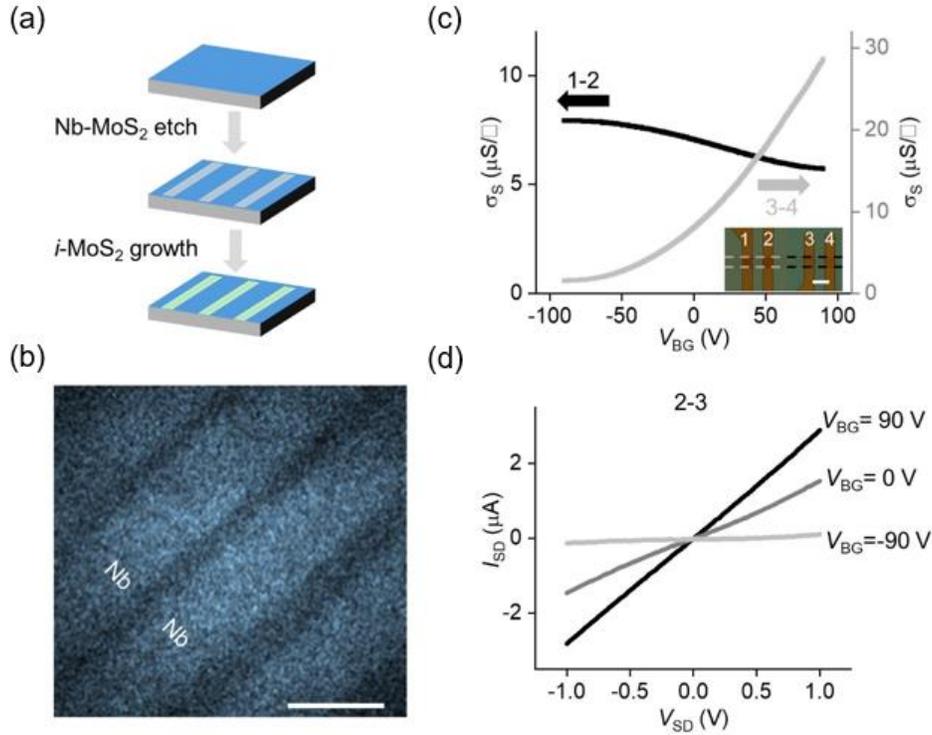


Figure 6.5 Nb-MoS₂ as metallic contacts. (a) Schematic of the patterned regrowth process using photolithography and Reactive Ion Etching. (b) XPS map of the Nb 3d peak for a representative Nb-MoS₂/*i*-MoS₂ lateral heterostructure. $C_{\text{Nb}} = 11\%$. Scale bar: 200 μm . (c) Corresponding transfer curves of the pre-patterned Nb-MoS₂ (1-2) and regrown *i*-MoS₂ (3-4). The inset shows the optical image of the device. Scale bar: 20 μm . (d) I - V curves for the electrical conduction across the heterojunction (2-3) at different V_{BG} .

6.6 Summary

In this chapter, we presented a direct application of our non-perturbative electrical measurement approach to precisely study the tuning of electrical conductivity in MoS₂ monolayers which are substitutionally doped. The electrical conductance σ_S of a Nb-doped MoS₂ monolayer is tuned over 7 orders of magnitude by controlling the dopant concentration, C_{Nb} . Our systematic study of the relationship between σ_S and C_{Nb} shows an exponential dependence between the two quantities, which can be explained by the smaller dielectric constant in 2D relative to that in the

bulk, resulting in a larger ionization energy. Furthermore, our study also demonstrates a general method for studying the effect of substitutional doping with different combinations of TMD materials where all the relevant energy levels and reduced Coulomb screening need to be considered together.

CHAPTER 7

FUTURE DIRECTIONS AND PERSPECTIVES

Until now, in this dissertation, we have discussed the following major achievements. First, we developed a non-perturbative electrical measurement approach suitable for surface-sensitive atomically thin semiconductors. This approach is enabled by two main techniques: one is the scalable direct laser patterning and the other is a polymer-free transfer of electrode onto the TMD surface over large areas. Second, we successfully probed the unintentional doping effects during conventional lithography and revealed that solvents like acetone play the most dominant role in tuning the conductivities of TMDs. Third, we demonstrated the controlled tuning of electrical conductivity of MoS₂ via substitutional doping during MOCVD and precisely measured the relationships between dopant concentration and sheet conductivity using the non-perturbative electrical measurement approach. Finally, the study of substitutional doping of monolayer MoS₂ revealed the crucial role of its reduced dimension and lower dielectric constant in governing the transport mechanism between the dopant sites which is starkly different than that in bulk semiconductors. Based on these, we can think of a few exciting future directions for 2D materials research.

7.1 Towards an All-van der Waals Integrated Circuitry

Van der Waals integration refers to the physical assembly of pre-prepared building blocks such as atomically thin materials, metal thin films, layers of dielectric oxide, etc. where the different layers interact with each other via vdW forces (Figure 7.1a). The main advantage of vdW integration is that it offers the relaxation of the need to integrate materials with lattice matching and processing compatibility. It can be applicable for generation of vdW stacks of materials with fairly different crystal structures and electronic properties (*e.g.*, metals, semiconductors,

insulators). Van der Waals integration of large-scale semiconducting monolayer TMDs into wafer scale heterostructures was demonstrated by our group in 2017. Figure 7.1b shows a representative cross-sectional image of a vertically stacked MoS₂/WS₂ superlattice.¹¹⁶ Besides, other examples of artificial heterostructures and superlattices with atomically clean and sharp interfaces between dissimilar materials such as graphene/Al₂O₃, MoS₂/Au, Bi₂Te₃/FeTe, CsPbBr₃/Au have also been demonstrated (Figure 7.1c).^{121,122} With these recent advances, one clear direction is to assemble gate dielectrics, contacts, semiconductors in order to realize all-vdW integrated atomically thin circuitry in the future (Figure 7.1d).

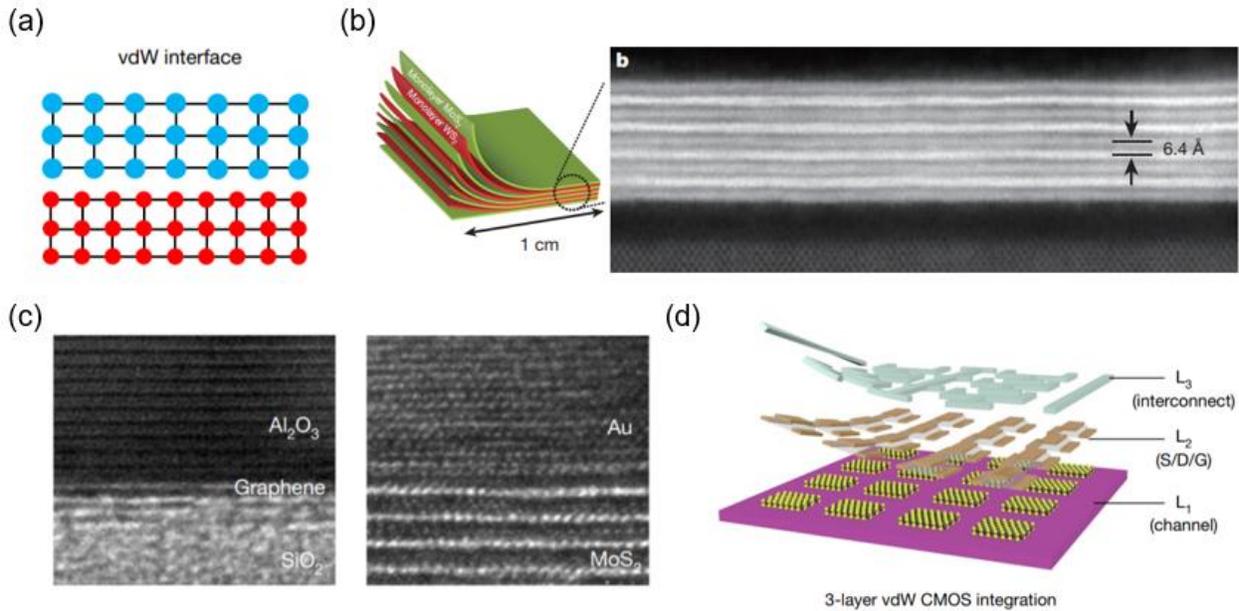


Figure 7.1 Van der Waals integrated interfaces and circuits. (a) Schematic illustration of bonding-free atomic structure at vdW interface. (b) Schematic of a vertically stacked MoS₂/WS₂ superlattice (left) and cross-sectional image of a superlattice film (right). (c) Cross-sectional image of vdW-contacting Al₂O₃/graphene interface (left) and Au/MoS₂ interface (right). (d) Schematic of a 3-layer vdW integrated circuit by assembling channel materials, electrodes and dielectrics building blocks. (a), (c), (d) adapted from Ref. 121 and (b) from Ref. 116.

Our non-perturbative measurement approach is an important step towards the goal as it integrates the semiconducting films and contacts via vdW interaction while keeping the channel pristine. This idea can be taken a step further if we consider patterning and stacking two or more

different TMDs and stack the electrodes on top of it. One way to make such TMD stacks is illustrated in Figure 7.2a. We show an alternate device fabrication scheme which can be referred to as the “*Template-strip lithography*”. The idea is to use metal templates to pattern the monolayer TMDs (Figure 7.2a). The metal (Au in our case) patterns are fabricated on a Si/SiO₂ substrate using photolithography and PMMA is spin-coated. The PMMA coated metal patterns with an attached thermal release tape (TRT) on top is dipped in potassium hydroxide, which will etch away

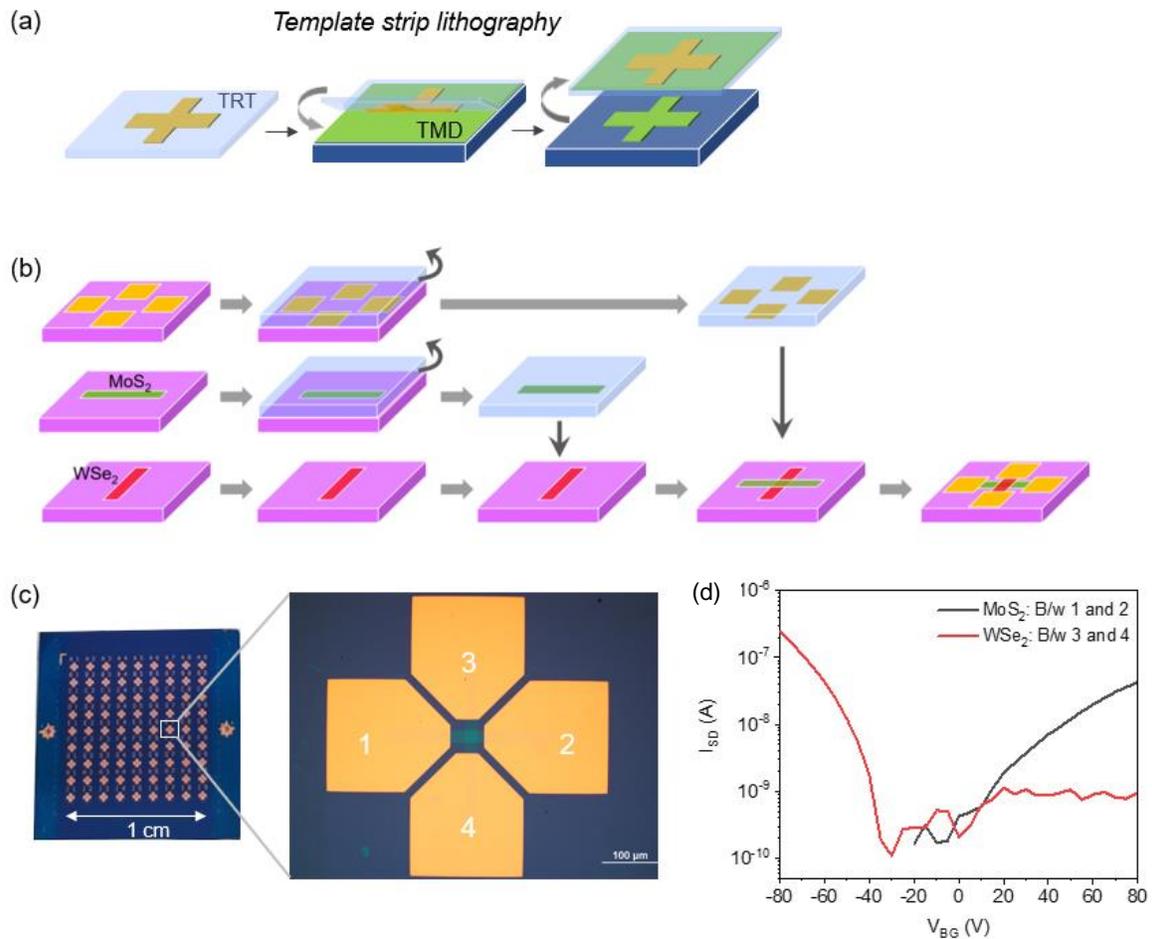


Figure 7.2 Template strip lithography for vdW integration. (a) Schematic of the template strip lithography for patterning monolayer TMDs using pre-fabricated metal templates. (b) Schematic of the fabrication process for making crossbar devices with stacked MoS₂ on WSe₂ as channels and stacked gold as contacts. (c) Photograph of crossbar device array over a centimeter length scale (left) and a magnified image of a device where MoS₂ connects the electrodes 1 and 2 while WSe₂ connects electrodes 3 and 4 (right). (d) Transfer curves obtained when measuring the current between different sets of electrodes showing the *n*- and *p*- type behavior when probing different sets of electrodes.

the substrate to produce a freely floating metal/PMMA/TRT template. The surface of metal, when functionalized in proper solvent, can enable us to modulate its adhesion with the TMD to allow the patterning of TMD. For example, perfluorodecanethiol tends to strongly adhere to the gold, in which case, the interaction of perfluorodecanethiol functionalized gold and TMD is weak. As a result, we can peel away the TMDs selectively, only from the areas that do not come into contact with functionalized gold, patterning the TMDs. In order to stack two or more TMDs, one of the TMDs patterned using template strip lithography can be patterned on the as-grown substrate. The other similarly patterned TMD layers can be peeled off of the substrate separately using PMMA and then stacked on top of it while ensuring the pristine interface between the TMDs (Figure 7.2b). The stacking can be carried out using our already developed vacuum stacking method in Ref. 116. Finally, after the polymer removal from the top of the TMD stack, the unfunctionalized Au/PMMA electrode template can be used to make the electrical contacts. We should note here that although in this case the metal contact templates were prepared by etching the substrate with patterned gold in potassium hydroxide, our non-perturbative electrode transfer can come handy at this stage which will minimize the number of steps. Furthermore, the non-perturbative electrode transfer method avoids the contact of metal surface with any chemicals and can enable us to stack metals which are susceptible to chemical damage. While a somewhat similar patterning of TMDs using gold assisted dry exfoliation was recently demonstrated¹²³, the contacts in this study is defined using evaporation and the device structure is not completely vdW integrated.

Figure 7.2c shows the result of our template strip lithography process. We generated *p-n* junction devices with vdW stacked monolayer MoS₂ on WSe₂ as the active channel and stacked gold electrodes as contacts. The batch fabrication of devices over a centimeter square area has been achieved. We indeed could control the conduction in the different layers by applying bias

between different electrodes (Figure 7.2d). WSe_2 that connects electrodes 3 and 4 exhibits a p -type transistor behavior whereas MoS_2 that connects electrodes 1 and 2, a typical n -type. One advantage of such patterning and stacking of TMDs is that it facilitates the control of conducting paths and the majority carriers along those paths. Figure 7.3a shows a schematic illustrating the design of two different conducting paths complementary to one another for n - and p -type transistors. By stacking monolayer WSe_2 on MoS_2 , both with complementary patterns, we are able to fabricate a device as shown in Figure 7.3b. The red and blue lines refer to the patterned MoS_2 and WSe_2 channels respectively and the electrodes are numbered for easier reference. The electrical data in

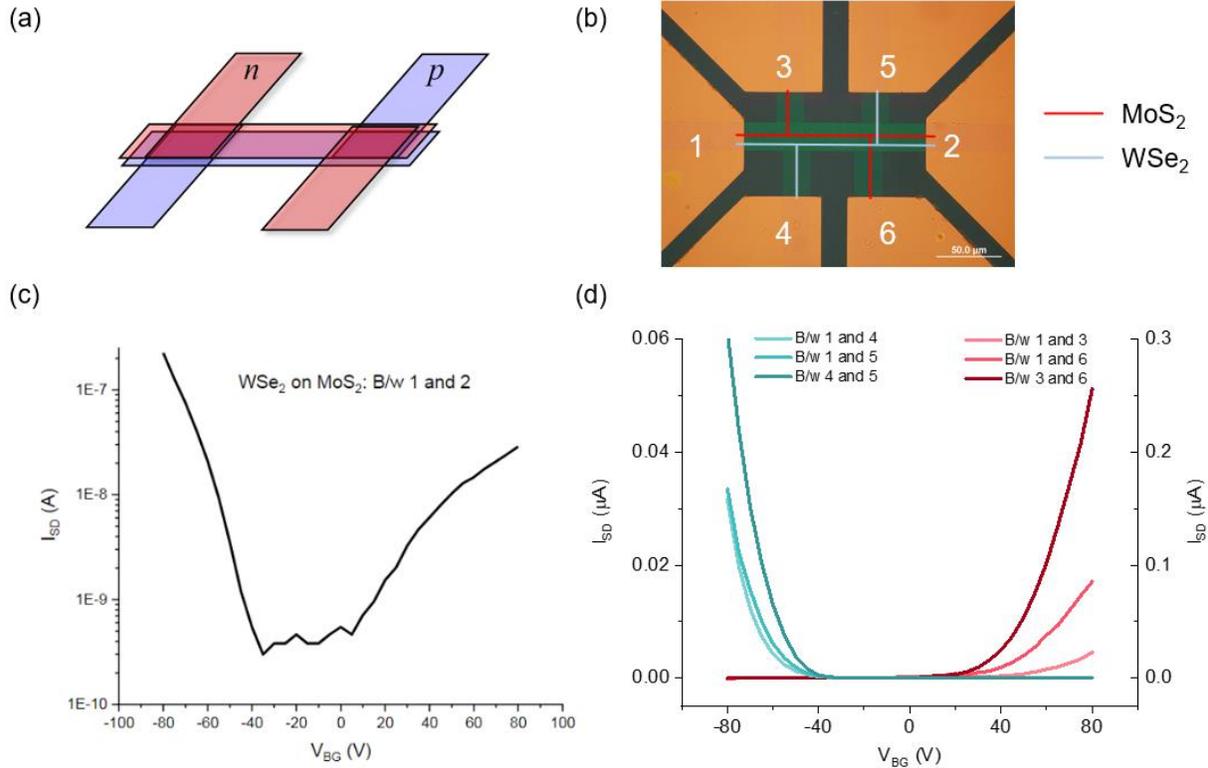


Figure 7.3 Designing of different conducting channels. (a) Schematic of stacked p - and n -type TMDs with complementary patterns. (b) Optical image of a device made using TSL with WSe_2 stacked on top of MoS_2 . The paths of the two are marked in blue (WSe_2) and red (MoS_2) lines, and the electrodes are designated numerically. (c) Transfer curve when electrodes 1 and 2 are probed. (d) Transfer curves when different pairs of electrodes are probed.

Figure 7.3c shows that when a bias is applied across the bilayer stack of TMDs the device exhibits an ambipolar behavior. The different conduction paths can be probed and the majority carriers can be tuned from electrons to holes as shown in Figure 7.3d.

So far, the vdW integration that we have achieved either by using template strip lithography or by the non-perturbative measurement method has focused on back gated devices. The use of a dielectric and a top gated geometry can further enhance the transport properties of the TMDs. However, the deposition of dielectric oxide using the commonly used approaches like atomic layer deposition, electron-beam evaporation or sputtering is known to introduce defects and damage in the case of graphene.¹²⁴ A similar consequence might be expected for atomic layer deposition of oxides on monolayer TMDs. Thus, a next future direction could naturally be to transfer the dielectric oxide on top of the channels and make top-gated devices.

7.2 Controlled Performance of TMD-based Devices and Sensors

One application of the non-perturbative measurement approach is making devices that require high sensitivity and low doping levels of the channel materials, *e.g.*, chemical sensors or biosensors.^{125,126} TMD-based gas sensors rely on detecting the change in electrical resistance of devices due to the gas/semiconductor surface interactions such as reduction/oxidation of the semiconductor, adsorption of chemical species directly on the surface and other surface chemical reactions. The high surface-volume ratios of 2D materials plays an important role in sensing applications. An example of MoS₂ monolayer chemical vapor sensor is shown in Figure 7.4, where it is used to detect analytes such as triethylamine, acetone, methanol and so on. Moreover, it exhibits much higher selectivity than the carbon nanotube-based sensors. One thing to note,

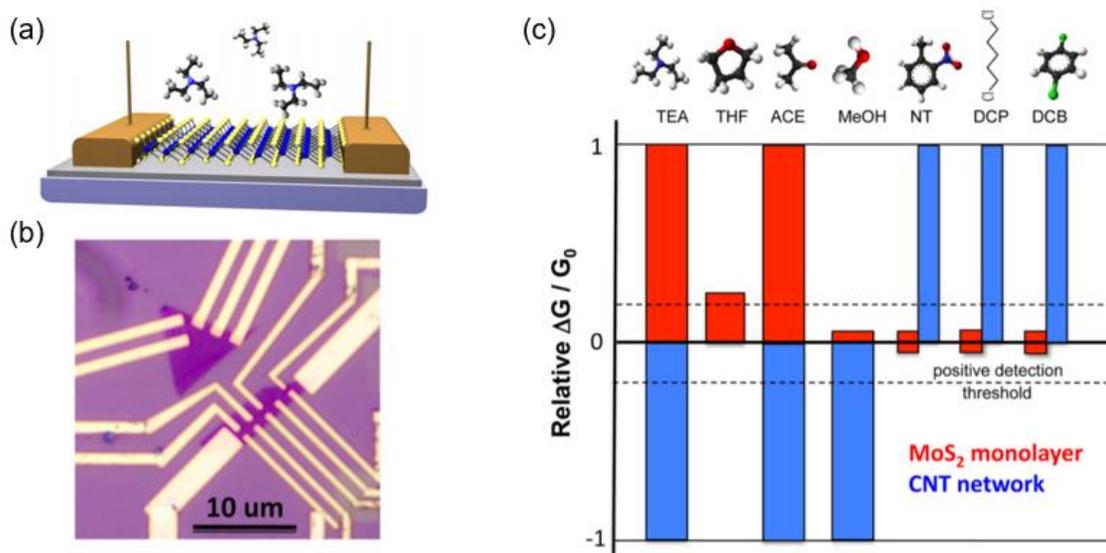


Figure 7.4 Chemical vapor sensing with monolayer MoS₂. (a) Schematic of a monolayer MoS₂ sensor. (b) An optical image of devices showing the monolayer MoS₂ flakes and contacted gold leads. (c) Histogram of MoS₂ and carbon nanotube-network sensor responses to various analytes. Triethylamine (TEA), tetrahydrofuran (THF), acetone, methanol, nitrotoluene (NT), 1,5-dichloropentane (DCP), and 1,4-dichlorobenzene (DCB). Reproduced from Ref. 125.

however, is that currently the device fabrication and electrical measurements are based on conventional lithography which can leave residues on the TMD surface and change their starting doping levels even before exposure to molecules. This is where our non-perturbative measurement approach can be applicable. The devices when measured non-perturbatively will preserve the pristine surface of TMDs and minimize any screening of interactions between the 2D surface and target molecules. Therefore, the electrical response of the sensors can be much higher and better controlled.

7.3 Patterning and Device Fabrication in Unconventional Environment

The field of 2D electronics can find applications for flexible and wearable electronics which are beyond the scope of 3D electronics. The bending stiffness of a material is proportional to the cube of the thickness and hence, the ultimate atomic level thickness of 2D materials make them an ideal system for foldable electronics. One of the prominent approaches to do so has been

to integrate devices on flexible substrates like polyimide, polyethylene terephthalate polymers.¹²⁷⁻
¹³⁰ It is interesting, however, to think of an application wherein the 2D integrated circuits can be folded to the nano-scale and injected to unconventional surroundings such as water or into biological systems to serve as sensors, detectors etc. This would require to push the limits of folding and for this, it is important that the circuits are entirely separated from the substrates. We have already demonstrated that inch-scale films of monolayer TMDs can be delaminated from the growth substrate onto a water surface without any polymer support.¹¹⁹ One option would be to directly make devices in unconventional environments like water and then control its mechanics to cause folding or movement in a controlled way. Keeping this in mind, we have made efforts to pattern the monolayer MoS₂ directly on water surfaces using the laser marker setup used earlier (Figure 7.5a). Figure 7.5 b-d illustrate this, where a delaminated MoS₂ on water-air interface can be ablated to produce desired patterns which diffuses on the water surface with time. Looking forward, we could delaminate MoS₂ with electrodes atop and then pattern it to define the channels as illustrated in Figure 7.5e. To realize a foldable integrated circuit that is stable in unconventional conditions can be an exciting future direction.

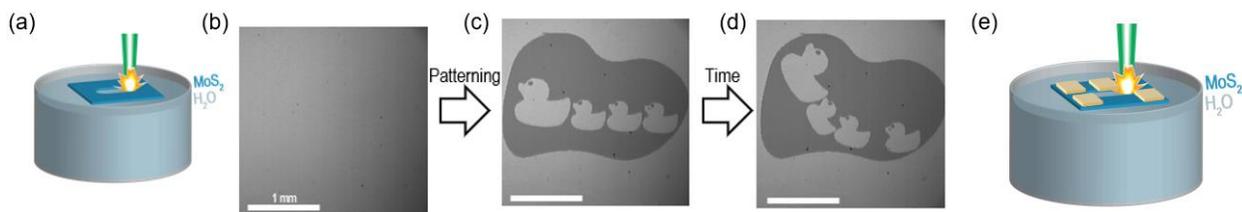


Figure 7.5 Patterning of 2D materials under unconventional conditions. (a) Illustration of laser patterning process on MoS₂ monolayer suspended at the water-air interface. (b-d) Images acquired for: (b) MoS₂ layer, floating on water following delamination from the growth substrate. (c) After patterning, demonstrating reproduction of the desired pattern. (d) After some time, the floating MoS₂ structures have diffused on the water surface. (e) Schematic illustration of laser patterning of monolayer MoS₂ with gold electrodes pre-deposited on their surface to define the conductive channels.

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