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Stretchable transistors and functional circuits for human-integrated electronics

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Electronics with skin- or tissue-like mechanical properties, including low stiffness and high stretchability, can be used to create intelligent technologies for application in areas such as health monitoring and human–machine interactions. Stretchable transistors that provide signal-processing and computational functions will be central to the development of this technology. Here, we review the development of stretchable transistors and functional circuits, examining progress in terms of materials and device engineering. We consider the three established approaches for creating stretchable transistors: buckling engineering, stiffness engineering and intrinsic-stretchability engineering. We also explore the current capabilities of stretchable transistors and circuits in human-integrated electronics and consider the challenges involved in delivering advanced applications.

Electronics is increasingly focused on connecting more and more objects for efficient information collection and exchange, ultimately creating an Internet of Everything. Collecting information from human bodies is central to the development of such ideas, and could lead to intelligent and ubiquitous healthcare[1], human/machine interfaces[2] and even advanced human capabilities[3]. However, this will require electronic devices that can be interfaced with various parts of the human body and that are capable of collecting signals with sufficient quality, resolution and stability. Such electronics need to have skin- or tissue-like mechanical form factors[4–6] and, in particular, should be capable of deforming to strains of tens of per cent without degradation in electronic performance.

Transistors will be central to the development of stretchable electronics, serving as the building-block elements in circuits for signal processing and computation. Imparting stretchability to transistors and then functional circuits is thus a key goal in achieving fully functional stretchable electronics (Fig. 1). The primary limitation is the lack of stretchable electronic materials[4,7]. To solve this issue, three general approaches have been established for imparting stretchability into transistors and circuits: buckling engineering, stiffness engineering and intrinsic-stretchability engineering. These approaches address the problem across all levels, from the entire electronic patch, to devices and down to the level of the component materials. They each have their own characteristics and advantages (Table 1), as well as distinct challenges for further developments.

In this Review, we first consider the working mechanisms and material components of transistors, then examine the three established strategies for creating stretchable transistors. We also explore the use of stretchable transistors and circuits in human-integrated electronics and consider the challenges involved in creating advanced capabilities towards next-generation electronics.

Basic knowledge and materials for field-effect transistors

There are two main types of field-effect transistor (FET): the junction field-effect transistor (JFET)[8] and the metal–oxide–semiconductor field-effect transistor (MOSFET)[9]. MOSFETs are more frequently used in integrated circuits (ICs) due to their large input impedance and compatibility with both depletion and enhancement modes. A typical MOSFET is a three-terminal device with three electrodes (source, drain and gate), a semiconducting channel and a dielectric layer. MOSFETs are further classified into two general types according to the geometry of the semiconducting channel: the conventional bulk type (Fig. 2a), fabricated on a single-crystal silicon wafer that serves as both the substrate and the bulk semiconductor layer[10], and the thin-film transistor (Fig. 2b), with a semiconductor thin-film layer deposited on a separate inactive substrate, which broadens the choice of semiconductor to emerging materials beyond silicon[11]. As such, there is now a rich library of semiconducting materials being used for transistors. These include germanium, III–V compounds[12] (such as GaN and GaAs), oxides[13] (such as indium gallium zinc oxide), carbon-based materials[14,15] (such as graphene and carbon nanotubes), transition-metal dichalcogenides[16] and conjugated organic molecules and polymers[17–19]. However, none of the high-performance semiconducting materials meet the requirements for stretchable transistors and circuits because of their rigid and fragile mechanical properties: that is, Young's modulus typically above 1 GPa and fracture strain typically below 5%. To achieve stretchable devices, innovations are thus required in materials and/or device design to impart stretchability either on the entire electronic circuit/system level or on the single-device level.

For the development of stretchable transistors (Fig. 2e), the overall goal is to combine skin-like stretchability (a strain level above 50%) with the high electrical performance of transistor devices, as well as the integration capability for circuit development, which is mainly subject to the device density, fabrication yield and performance uniformity. The key figures of merit for the electrical performance of transistors (Fig. 2c,d) are the threshold voltage (V_T), subthreshold swing (SS), on/off ratio (I_{on}/I_{off}), transconductance (g_m) and the cutoff frequency (f_T)[20]. V_T represents the gate-voltage boundary that switches a transistor between open-circuit (off) and short-circuit (on) states. SS quantifies how fast such switching takes place in the subthreshold region. Lower V_T and smaller SS are key to achieving low power consumption. For digital applications mainly based on transistors switching between on and off states, the ratio I_{on}/I_{off} needs to be sufficiently high, typically $>10^4$. For analogue applications, g_m is the key figure of merit, describing how effectively

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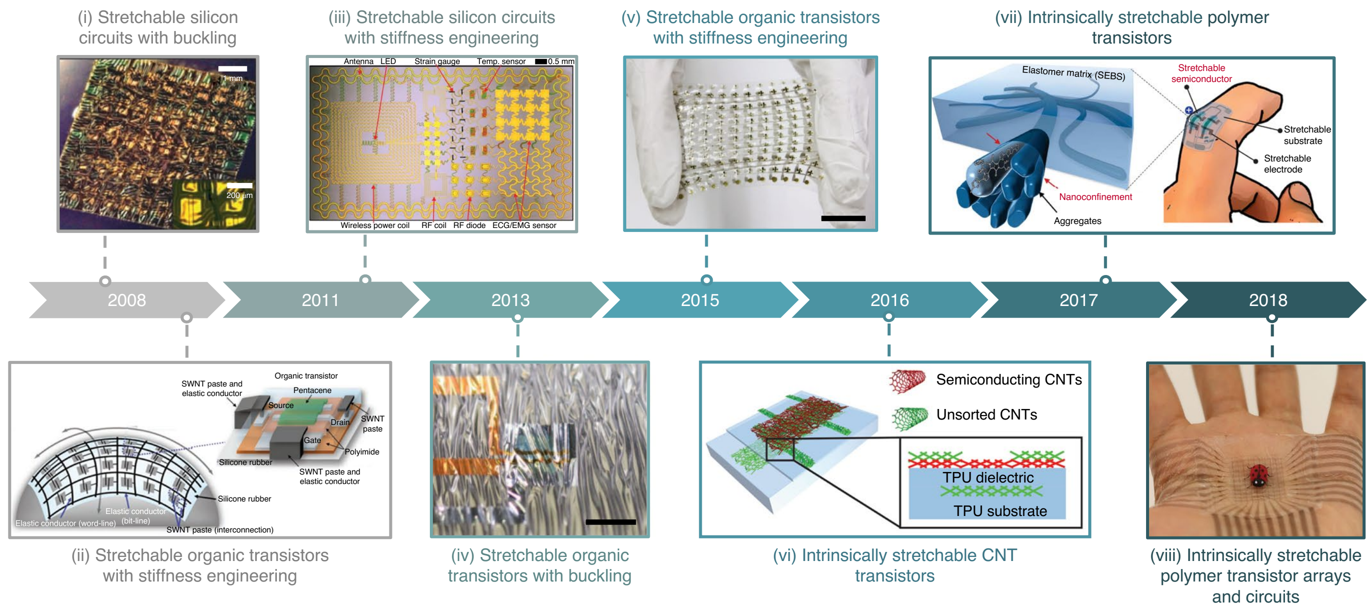

Fig. 1 | Evolution of stretchable transistors and functional circuits. From left to right: (i) stretchable silicon circuits (2008); (ii) organic field-effect transistor (OFET) active matrix (2008); (iii) stretchable epidermal electronics (2011); (iv) stretchable OFET (2013); (v) stretchable OFET active matrix (2015); (vi) stretchable CNT-based transistor (2016); (vii) intrinsically stretchable OFET (2017); (viii) stretchable OFET active matrix (2018). TPU, thermoplastic polyurethane. Scale bar in (v), 20 mm. Figure adapted with permission from: (i), ref. [22], AAAS; (ii), ref. [47], AAAS; (iii), ref. [86], AAAS; (iv), ref. [23], Springer Nature Ltd; (vii), ref. [62], AAAS; (viii), ref. [74], Springer Nature Ltd. Figure reproduced with permission from: (v), ref. [45], Springer Nature Ltd; (vi), ref. [54], Wiley.

the gate voltage (V_G) modulates the drain current (I_D), which is defined as

$$g_m = \frac{dI_D}{dV_G} = \begin{cases} \frac{W}{L}\mu C_i V_D & \text{when } V_D < V_G - V_T \\ \frac{W}{L}\mu C_i (V_G - V_T) & \text{when } V_D > V_G - V_T \end{cases}$$

where W and L are the channel width and length respectively, μ is the charge-transport mobility, C_i is the gate dielectric capacitance per unit area and V_D is the drain voltage. Finally, the dynamic performance of transistors for processing alternating current signals is evaluated by the cutoff frequency f_T for effective switching, which is given by

$$f_T = \frac{g_m}{2\pi C_G} \cong \begin{cases} \frac{\mu V_D}{2\pi L(L+2L_{ov})} & \text{when } V_D < V_G - V_T \\ \frac{\mu (V_G - V_T)}{2\pi L(L+2L_{ov})} & \text{when } V_D > V_G - V_T \end{cases}$$

Here, C_G is the total gate capacitance, which is given by $C_G = C_{ch} + 2C_{ov} \cong C_i W(L + 2L_{ov})$, where C_{ch} is the channel capacitance, C_{ov} is the parasitic gate-overlap capacitance and L_{ov} is the gate-overlap length with drain/source electrodes.

The physical origins of these figures of merit suggest the following electrical-performance-relevant requirements for the development of stretchable transistors (Fig. 2e): semiconductors with high μ; dielectrics with high dielectric constant κ; optimized semiconductor/dielectric interfaces; miniaturized device sizes from improved fabrication processes and optimized electrode/semiconductor contacts. For integration into functional circuits, stretchable transistors are also subject to the requirements of sufficiently high device density, fabrication yield and performance uniformity (Fig. 2e).

When moving transistors to stretchable designs, the fundamentals of device physics would need to incorporate the influences of applied strains, so that the evolvement of the transistors' performance under stretching could be predicted. For the engineering strategies (that is, stiffness engineering and buckling engineering) that exert a minimal level of strain on the transistor devices, the device performance is not affected by strain. However, when the applied global strain goes beyond the threshold value set by the least stretchable component in the overall designs, device failure usually happens as a result of a broken component and/or a delaminated interface. In contrast, for transistors that operate under strains through intrinsic stretchability, an in-depth understanding of the influence of strain on the device performance is highly needed, which, for the above-described figures of merit, can be divided into two aspects: the influences on the material parameters (including μ of the semiconductor, C_i of the gate dielectric and conductivity of the electrodes), which could come from the changes of a certain material's structural morphology and/or layer-to-layer interface morphology; and the influences on the device geometric parameters (including W and L).

Buckling-engineering-enabled stretchable transistors and circuits

Before research into stretchable electronics began, extensive efforts had been made in the development of flexible electronics[21] that can undergo bending–unbending deformations. These developments laid an important foundation for one of the strategies for realizing stretchable electronics, which is to convert in-plane stretching to out-of-plane unbending deformation through a buckled structure (Fig. 3a). Beginning with this mechanical behaviour, the buckling engineering method was devised as a generally applicable strategy for making stretchable transistors from almost any material that can be fabricated into flexible thin films.

In general, the formation of buckled structures can be realized by several methods, including pre-stretch–release[22,23], compression[24], moulding[25,26], solvent swelling[27], thermal expansion[28] and 3D printing[29]. Among these, the pre-stretch–release and moulding methods have been adopted the most for building stretchable transistors. In the pre-stretch–release method[22,23], flexible thin films are first fabricated on rigid substrates and then transferred onto a pre-stretched

Table 1 | Comparison of stretchable transistors based on three general approaches and traditional silicon technology

		Buckling engineering	Stiffness engineering	Intrinsic-stretchability engineering	Silicon-based integrated circuits
Material requirements	Semiconductors	Nearly all the semiconductors	Nearly all the semiconductors	Conjugated polymers; semiconducting CNT networks	Single-crystal silicon
	Dielectrics	Nearly all the dielectrics, high-κ dielectrics are mostly used	Nearly all the dielectrics, high-κ dielectrics are mostly used	Elastomers or elastomer composites	SiO_2, Si_3N_4
Fabrication	Key process	Transfer printing; buckles generation	Transfer printing; bonding between rigid island and stretchable substrate	Layer-on-layer deposition and patterning	Deposition, oxidation, metallization, lithography
	Yield	Medium	Low	High	Ultrahigh
Electrical performance	Mobility ($cm^2\,V^{-1}s^{-1}$)	290 (n-type silicon[22]); 140 (p-type silicon[22]); 10 (CNT[31]); 40 (graphene[25]); 0.88 (organic semiconductor[23])	370 (n-type silicon[35]); 130 (p-type silicon[35]); 0.48–1.8 (organic semiconductor[45,47])	27 (CNT[54]); 0.1–2 (polymer semiconductor[55,62])	1,000 (n-type); 450 (p-type)
	Operation voltage	Low (1–10 V)	Low (1–10 V)	High (10–30 V)	Very low (<1 V)
Integration capability	Channel length	100–200 μm (refs. [22,23,25])	200–500 μm (refs. [35,45])	50–200 μm (refs. [60,62,74])	7 nm
	Device density (cm^{-2})	Up to 280 (ref. [22])	Up to 400 (ref. [35])	Up to 347 (ref. [74])	Over 10 billion
Stretchability	Highest stretchability	~5% for silicon[22]; ~20% for CNT[31] and graphene[25]; ~100% for organic semiconductors[23]	~100%[35,45]	Up to 600%[62]	Non-stretchable
	Strain distribution	In-plane strain is converted to out-of-plane local bending	Not uniform, the strain is mostly taken by the interconnects	Uniform	
Suitable applications		Analogue signal conditioning, digital computations	Digital computations	Sensing, multiplexing, analogue signal conditioning	Multiplexing, analogue signal conditioning, digital computations

elastomeric substrate. The release of the stretching causes the film to buckle. In the moulding method[24,25], the buckled structures are built into a thin film by depositing it onto substrates with a wavy surface.

Buckling engineering on functional materials. Buckling engineering can be adopted to introduce stretchability into non-stretchable functional layers, which can be further integrated into stretchable devices. This has been demonstrated with single-crystal silicon. By transferring microfabricated single-crystal silicon ribbons onto a pre-stretched elastomeric substrate and then releasing the substrate, the resulting wavy structures (Fig. 3b, top) can accommodate 10% stretching on the elastomer substrate[30]. Using this method, stretchable transistors have been realized by incorporating other functional layers (metals and dielectrics) before buckle formation. In addition to conferring stretchability to rigid materials, the pre-stretch–release process can also serve to increase the stretchability of moderately stretchable layers. For example, the stretchability of semiconducting single-walled carbon nanotube (SWCNT) films can be effectively increased by buckle formation during repeated stretching and releasing steps[31].

The moulding method — the other buckling approach that is easy to implement — has also been applied to functional materials[25,26]. One representative example was made using an Al_2O_3 thin film, one of the most widely used high-κ dielectric materials, by depositing it on rough copper foils (Fig. 3b, bottom). By incorporating the buckled Al_2O_3 with graphene as the semiconductor, the obtained transistor achieved a stretchability of 20%[25].

Buckling engineering on full devices. The buckling method can also be applied directly to completed transistor devices fabricated on flexible substrates[22,23]. This allows the transistor fabrication process to be decoupled from the buckle formation processes, so that any type of flexible transistor[23] — even circuits[22] — can operate with global strain applied to the elastomeric substrates. For example, the pre-stretch–release method has been utilized to fabricate buckled silicon complementary metal–oxide–semiconductor (CMOS) circuits[22]. To reduce the maximum bending-induced strain on non-stretchable layers, those layers were made to be thin and were placed closer to the mechanical neutral plane. As a result, such CMOS circuits can maintain unaltered performance with 5% global strain (Fig. 3c, top) and are able to preserve their performance after 30 stretching cycles.

To further increase the stretchability of devices, a greater amount of buckling needs to be introduced, but the bending-induced tensile/compressive strains should not exceed the fracture onset strains of any of the material components. Hence, the improvement in stretchability can be achieved by using materials with larger fracture strains. A state-of-the-art work implemented this strategy by

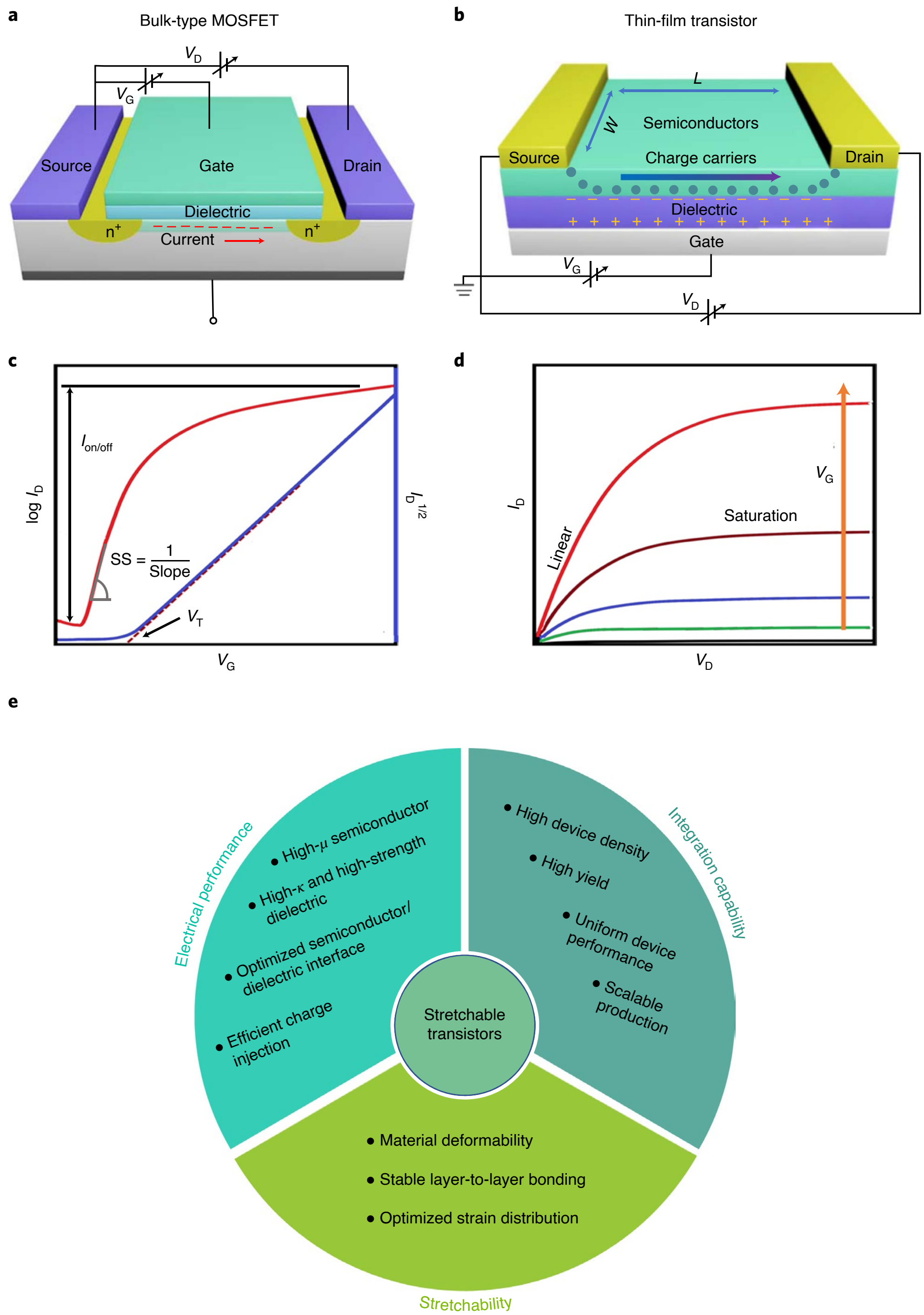

Fig. 2 | Schematic representations of transistor structures and the transfer and output characteristic curves. a, A conventional bulk-type MOSFET. **b**, A thin-film transistor. **c**, A typical transfer curve of the transistor. Key figures of merit, including threshold voltage (V_T), subthreshold swing (SS) and on/off ratio ($I_{on/off}$), are shown. **d**, A typical output curve of the transistor. **e**, Performance metrics in the development of stretchable transistors.

using organic semiconductors as the transistor channel layer and sandwiching the functional devices between two ultrathin polymer foils[23], enabling a global stretchability of 233%. Moreover, the device shows nearly unaltered performance under 100% strain for over 200 cycles and can be operated at high temperatures and in aqueous environments (Fig. 3c, bottom).

Perspective. In general, the most prominent advantages of the buckling engineering method are its simplicity in execution and its broad applicability to large groups of materials and device structures. Additionally, electrical performance is almost completely decoupled from the mechanical deformations because of the low level of bending-induced strain. However, as the buckling formations are stochastic processes in each of the releasing processes, the bending-induced maximum strains at the microscopic scale could have some variations among different releasing cycles[32]. Multicycle stretching robustness thus needs to be studied further, both experimentally and theoretically. Furthermore, buckling

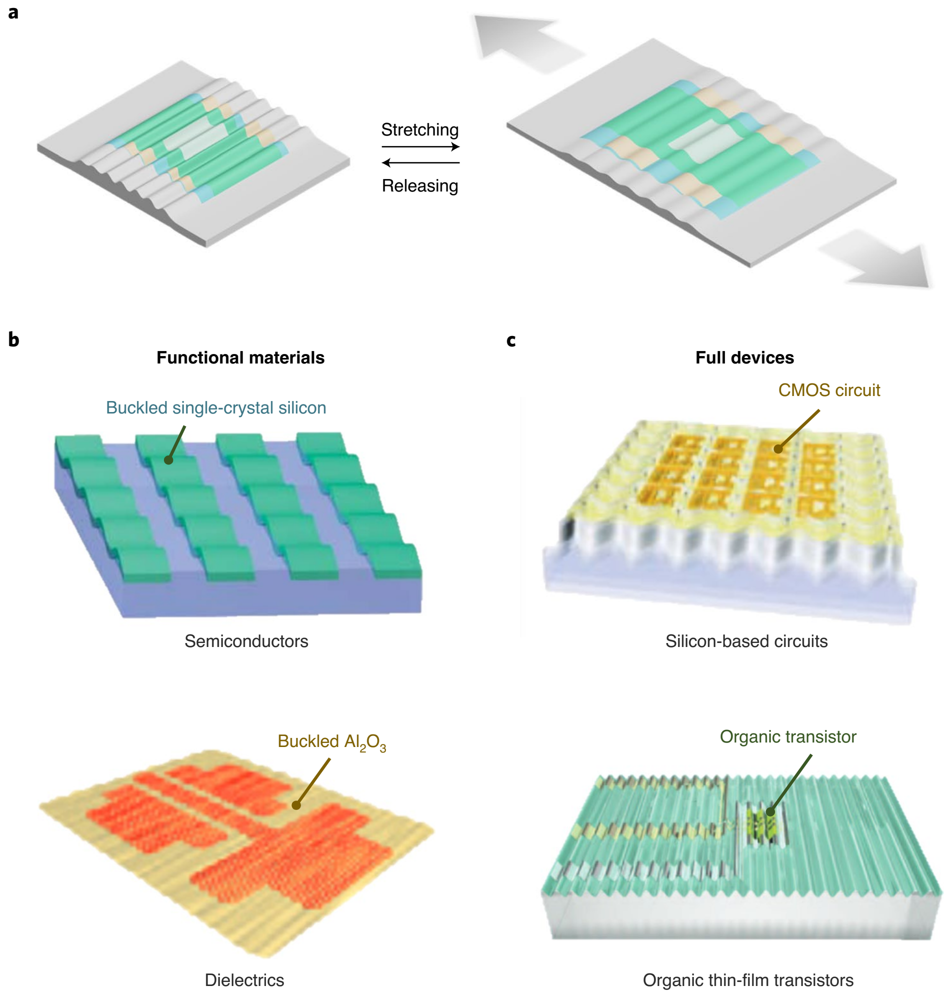

Fig. 3 | Buckling-engineering-enabled stretchable transistors and circuits. a, Schematics of the stretchability enabled by buckling engineering. **b**, Buckling engineering on functional materials for stretchable transistors: buckled single-crystalline silicon prepared by the pre-stretch–release method (top); buckled Al_2O_3 prepared by moulding on rough copper foils (bottom). **c**, Buckling engineering on full devices: buckled silicon CMOS circuits (top); buckled organic thin-film transistor (bottom). Figure reproduced with permission from: **b** (top), ref. [30], AAAS; **b** (bottom), ref. [25], Springer Nature Ltd; **c** (top), ref. [22], AAAS; **c** (bottom), ref. [23], Springer Nature Ltd.

engineering often leads to roughened device surfaces and usually needs relatively thick substrates, which can be a challenge for forming intimate interfaces with biological tissues. Additionally, for applications that require transparency in devices (for example, photodetectors), the buckled configuration could interfere with light penetration. More innovations in device design are desired to mitigate these side effects. Also, to enable scalable fabrication of transistor arrays, innovations are required to achieve a uniform large-scale buckling-formation process.

Stiffness-engineering-enabled stretchable transistors and circuits

In general, circuit systems are spatially heterogeneous, with three types of area: functional-device-occupied areas, conductive-interconnect-occupied areas and empty spacing areas. To impart global stretchability, there is plenty of mechanical-engineering space that can be explored for varying the strain dissipation pattern among these different types of area. As such, stretchability can be imparted to functional devices through appropriate mechanical designs that dissipate most of the applied strain into the empty and interconnect areas, leaving the functional devices experiencing minimal strain (Fig. 4a). In this way, stretchability is only a demand for conductors that serve as interconnects.

From solid mechanics, when a strain is applied onto a continuum object, the generated local strain is inversely proportional to the local stiffness[33]. Therefore, the strain applied to functional devices can be effectively reduced by increasing the stiffness of the device regions. This stiffness engineering has become another major approach that can enable the use of non-stretchable devices to achieve stretchable circuits. However, it should be noted that such non-uniform strain distribution in a mechanically heterogeneous structure is typically accompanied by the generation of large stresses at soft/stiff boundaries. As a result, the system-level stretching robustness largely relies on strong adhesion at such boundaries.

Stretchable conductors as interconnects. As described above, having stretchable conductors is crucial for realizing the stiffness engineering approach. Conventionally, metals have been the only class of materials serving as conductors in electronics. Certainly, there are liquid-phase metals (for example, mercury, gallium-based alloys) with intrinsic ductility (Fig. 4b(i)) that have been extensively explored for their use in stretchable electronics[34]. However, due to

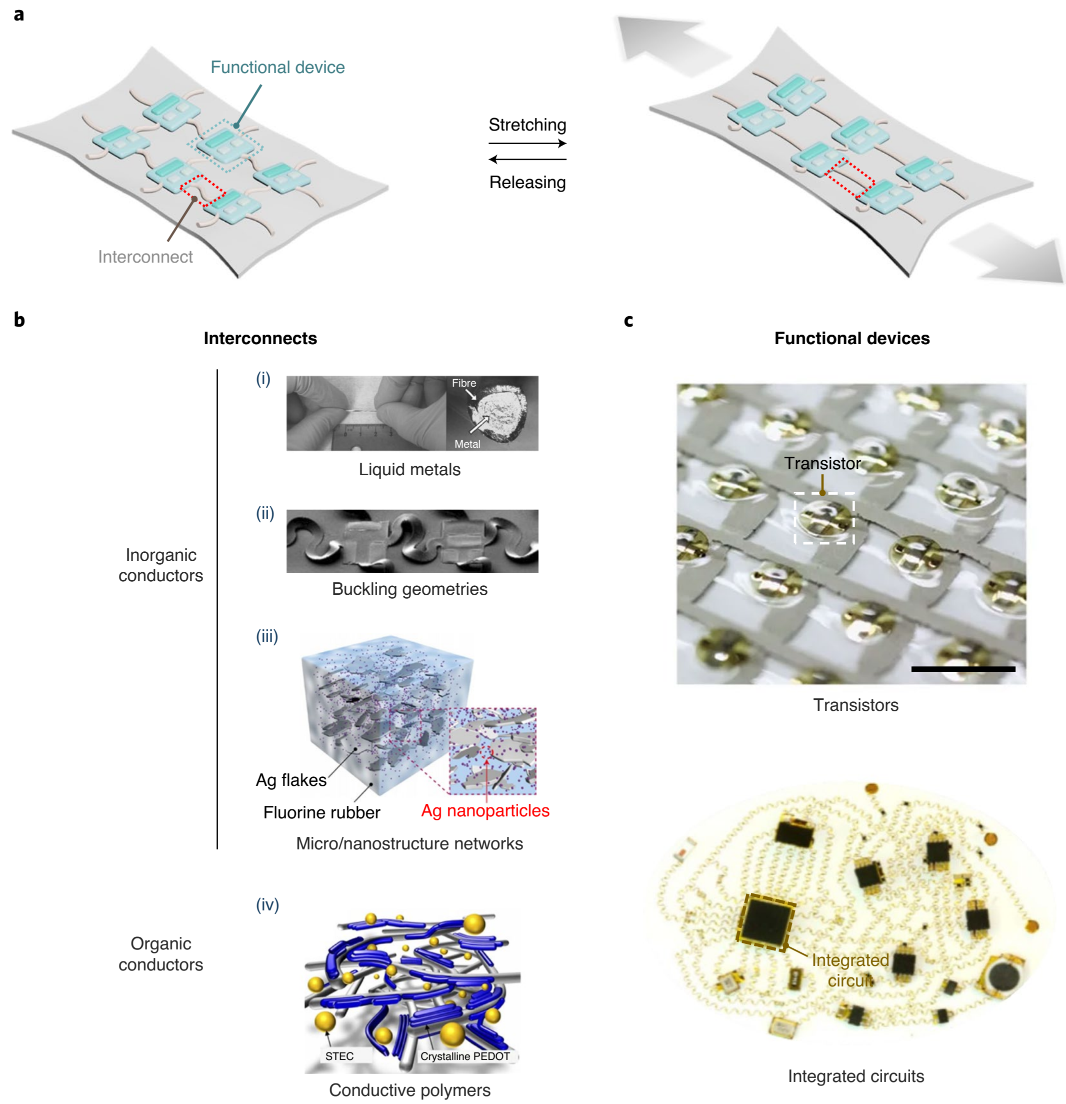

Fig. 4 | Stiffness-engineering-enabled stretchable transistors and circuits. a, Schematics of the stretchability enabled by stiffness engineering. **b**, Stretchable interconnects that dissipate major strain under global stretching: (i) liquid metal with inherent stretchability; (ii) metals with buckling geometry; (iii) micro/nanostructure network composed of Ag nanoparticles/nanosheets and elastomers; (iv) highly stretchable conductive polymer prepared by blending PEDOT:PSS with plasticizers. STEC, stretchability and electrical conductivity (STEC) enhancers. **c**, Functional devices as 'rigid islands': as-fabricated transistors (top; scale bar, 5 mm); chip-scale ICs (bottom). Figure reproduced with permission from: **b**(i), ref. [87], Wiley; **b**(ii), ref. [35], copyright (2008) National Academy of Sciences, USA; **b**(iii), ref. [39], Springer Nature Ltd; **b**(iv), ref. [41], reprinted with permission of AAAS, © The Authors, some rights reserved; exclusive licensee AAAS. Distributed under a Creative Commons Attribution NonCommercial Licence 4.0 (CC BY-NC); **c** (top), ref. [45], Springer Nature Ltd; **c** (bottom), ref. [50], Springer Nature Ltd.

their structural instability compared with solid-state materials, challenges arise when trying to use them to build devices with both miniaturized size and long-term stability. As such, many engineering efforts and breakthroughs have been made to impart stretchability to solid-state metals and other conductors[7], mainly through the design of strain-dissipative geometries, including buckling structures and micro/nanostructure networks. For the buckling geometry, not only the out-of-plane buckling reviewed above, but also in-plane buckling designs (for example, serpentine designs) have proven to be effective for generating stretchability up to 100%[35] (Fig. 4b(ii)). In parallel, micro/nanostructure networks can also deform to large strains without breaking the conducting percolations (Fig. 4b(iii)), which is similar to the deformability in kirigami structures[36]. Because the structural regularity in kirigami patterns is not an essential requirement for deformability, micro/nanostructure networks can be built by some simple approaches, including the formation of microcracks during initial stretching[37] and the assembly of pre-synthesized conductive nanostructures (for example, Ag nanowires[38], Ag nanoparticles/flakes[39] and CNTs[40]).

More recently, conductive polymers, such as poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) that is inherently rigid and brittle due to its high crystallinity, have been successfully engineered to be stretchable through blending with plasticizers[41] and/or surfactants[42], as well as by the engineering of processing conditions[43]. Representatively, the plasticizer-blending method (Fig. 4b(iv)) has achieved the highest ever stretchability up to 600% strain[41]. For more detailed discussions about stretchable conductors, there are several recently published review papers particularly focused on this topic[7,44].

Functional devices as rigid islands. With the stiffness engineering approach, almost any type of transistor can, in principle, be used for stretchable electronics. To achieve this, transistors are usually fabricated on patterned flexible supporting layers (for example, polyimide) and then placed onto elastomeric substrates, as isolated islands. The increase in local stiffness is provided by either the flexible supporting layer[35] or surrounding elastomeric substrates with increased crosslinking density[39,45]. This design concept has been successfully applied to thin-film transistors built with a variety of semiconductors, including silicon[35,46] and organic small molecules (for example, pentacene[47] and dinaphthothienothiophene (DNTT)[45]) (Fig. 4c, top). These have demonstrated mobility values in the range of 0.1–1 $cm^2 V^{-1} s^{-1}$. By applying stiffness engineering designs to single-crystal silicon CMOS transistors[35], mobilities up to 100–400 $cm^2 V^{-1} s^{-1}$ at 100% strain can be provided. Meanwhile, such devices remain stable after being stretched for over 1,000 cycles. The key fabrication innovations for building such systems include the creation of single-crystal silicon nanoribbon structures[30] and the physical transfer of these silicon nanoribbons onto a flexible substrate[48]. However, such multiple physical transfer steps cause challenges for achieving high yield and alignment resolution.

With its very loose requirements in terms of transistor form factors for achieving global stretchability, the stiffness engineering approach has also enabled the integration of commercial IC chips into stretchable electronics (Fig. 4c, bottom). However, the rigid and bulky nature of IC chips makes it challenging to achieve stable bonding between the hard chips and the adhered stretchable substrate under large strains. This can be resolved by adding support posts on elastomeric substrates for chip bonding[49] and/or by embedding chips in a soft medium[50]. More recently, to further increase the device density for more advanced functions, three-dimensional (3D) stacking of multiple chip-bonded stretchable layers has been realized[51]. This approach allows the possibility of using state-of-the-art electronic components to realize fully functional and stand-alone stretchable electronic systems.

Perspective. Up to now, most advanced applications of stretchable electronics have been realized by stiffness engineering approaches[49,51]. An important advantage of this, worth noting here, is that the electrical functions are almost completely decoupled from the stretching until mechanical failure (for example, delamination or fracture) is reached. For further enhancement of the stretchability, investigations and optimizations are needed to achieve the following: (1) more robust mechanical designs for stretchable systems to allow for tolerance-unpredicted strain distributions arising from possible fabrication non-uniformities and (2) stronger adhesion between soft and hard interfaces. More specifically, fabrication using elemental transistors faces the challenges of improving the fabrication yield and transistor density, whereas the use of IC chips typically gives rise to bulkier devices, for which special designs are needed to build intimate skin/tissue interfaces. Overall, because certain human-integrated applications require not only global stretchability but also other favourable mechanical properties (for example, softness and local deformability), in-depth investigations are needed to assess the suitability of stiffness-engineered systems for such applications.

Intrinsically stretchable transistors and circuits

High performance and good integration capability are the two main aspects of requirements for transistors. The two device-level strategies for imparting stretchability discussed above can preserve the inherent electrical performance of materials and devices, but inevitably sacrifice integration capability, which is determined by the fabrication yield, device density and uniformity. These limitations can be bypassed by utilizing a fundamentally different approach (Fig. 5a), that is, to impart stretchability as an intrinsic property to electronic materials (semiconductors, conductors and dielectrics), while maintaining their original functionalities.

Structurally, a material's stretchability can only be obtained from loosely packed structures. Such structures are commonly found in polymers[52], making them a promising material family for providing inherent stretchability. Other than this, the percolated networks of 1D nanostructures can also render thin films with macroscopic continuity and stretchability[53], as discussed in the last section. Hence, for the development of intrinsically stretchable semiconductors, conjugated polymers[19] and 1D nanomaterials (for example, CNTs[54]) with semiconducting properties emerge as the two major avenues.

Intrinsically stretchable semiconductors. Extensive research efforts in the past 40 years have led to the development of conjugated polymers with charge-carrier mobility in the range of 1–10 $cm^2 V^{-1} s^{-1}$, which rivals that of poly-silicon[17]. However, those high-mobility polymers still have very limited stretchability due to their typical planar backbone architectures and relatively high crystallinity. Because large mechanical deformability can only be afforded by disordered and loosely packed structures, the main challenge for achieving intrinsically stretchable polymer semiconductors is to moderately reduce the chain ordering and packing, without affecting the charge-transport properties. Generally, this challenge can be addressed by the following three engineering strategies: backbone engineering, side-chain engineering and morphological engineering.

Towards achieving a more flexible polymer chain to obtain high deformability, the demonstrated backbone engineering approaches (Fig. 5b(i), left) include building random copolymers[55], incorporating soft segments[56,57] and introducing backbone torsions[58]. Among these, incorporating soft segments has been explored the most. One representative design incorporates alkyl segments, carried out through either block copolymer[56] or conjugation spacer approaches[57]. More recently, the backbone engineering strategy was further extended to the incorporation of supramolecular interactions[59] (that is, dynamic bonds) between backbones (Fig. 5b(i), right) to dissipate strain energy. However, these backbone modifications to some extent affect charge-carrier delocalization along or across the polymer, thus sacrificing charge-carrier mobility.

Compared with the modifications on backbones, engineering side chains with bulky and/or soft segments (Fig. 5b(ii), left) could serve to increase the stretchability by weakening the interactions between polymer chains while having less influence on the electrical performance. Synthetically, such side-chain modification can be implemented during monomer synthesis[60] or through post-polymerization attachment[61]. One representative example is an isoindigo-based conjugated polymer modified with the bulky carbosilane side chain[60] (Fig. 5b(ii), right), which gained a stretchability of 100% strain while still providing mobility above 1 $cm^2 V^{-1} s^{-1}$.

Despite the high structural tunability provided by the backbone and side-chain engineering methods, these synthetic approaches can be technically complicated. Opportunities also lie in the physical engineering of polymer morphologies via the processing conditions so as to enhance the chain dynamics[62–65] (Fig. 5b(iii), left). Along this line, we recently created a facile and versatile approach based on the nanoconfinement effect[62]. By simply blending a conjugated polymer with an elastomer (Fig. 5b(iii), right) to enable nanoscale phase separation, a percolated nanoconfined morphology could be achieved. The afforded nanoconfinement effect enabled a stretchability of over 100% strain without affecting the charge-carrier mobility. Moreover, this approach was shown not only to be broadly

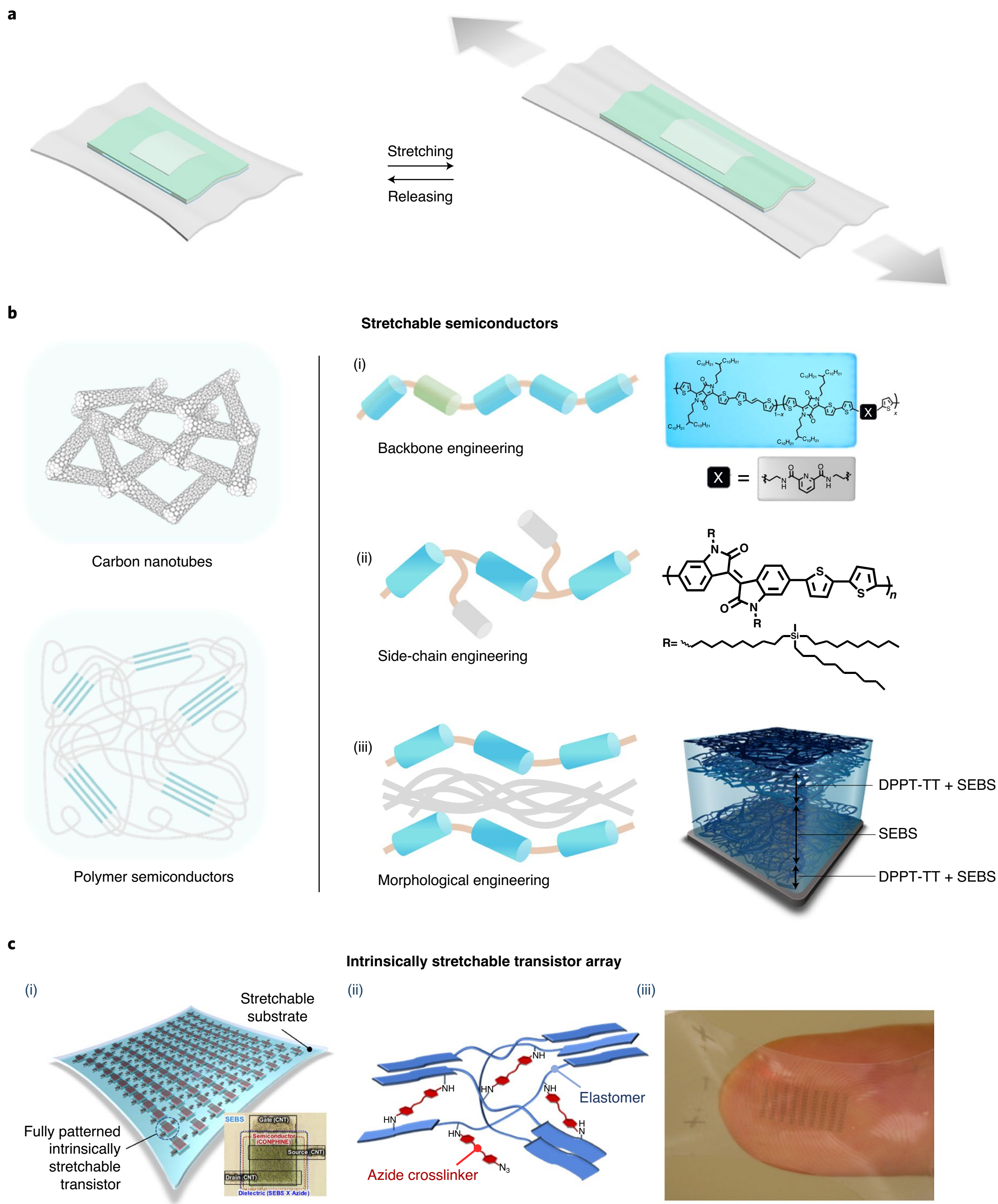

Fig. 5 | Intrinsically stretchable transistors and circuits. a, Schematics of intrinsically stretchable transistors. **b**, Schematics of typical stretchable semiconductors and general strategies for designing stretchable polymer semiconductors: (i) backbone engineering (left) and a diketopyrrolopyrrole (DPP)-based polymer semiconductor with PDCA modified backbone (right); (ii) side-chain engineering (left) and an isoindigo-based polymer semiconductor modified with a bulky carbosilane side-chain structure (right); (iii) morphological engineering (left) and a stretchable polymer semiconductor prepared by blending DPPT-TT with SEBS (right). **c**, Scalable fabrication of an intrinsically stretchable transistor array: (i) schematics of the intrinsically stretchable transistor array and magnified image of one transistor in the array; (ii) a direct photo-patterning process for dielectrics; (iii) an intrinsically stretchable transistor array on the fingertip, with device density of 347 cm^{-2}. Figure reproduced with permission from: **b**(i) right image, ref. [59], Springer Nature Ltd; **b**(ii) right image, ref. [60], American Chemical Society; **c**, ref. [74], Springer Nature Ltd. Figure adapted from: **b**(iii) right image, ref. [62], AAAS.

applicable to a variety of conjugated polymer structures, but also to demonstrate excellent shelf stability. More recently, this nanoconfinement design has been combined with a solution-shearing method to achieve multiscale ordering, which further enhances the mobility[66]. Several other polymer-physics-originated concepts have also been created for engineering stretchability[63,64].

Although polymer semiconductors are promising materials with excellent inherent stretchability, it should be noted that the morphologies of polymer films can evolve during repeated strain cycles, which might present a challenge for achieving unaltered electrical performance from such films during repeated stretching. For example, a slight increase in the roughness of a polymer film has been observed during multiple stretch–release cycles, contributing to a gradual decrease in mobility[62]. On the other hand, because of the typical high stretchability of the functional layers, intrinsically stretchable transistors can better avoid a complete loss of function as a result of repeated stretching.

Besides conjugated polymers, SWCNTs have also been explored as a material system for the development of stretchable semiconductors. In contrast to polymer semiconductors, SWCNTs form percolated networks to transport charges, and their stretchability comes from the reorientation and sliding of individual tubes[53]. CNT networks, with macroscopic charge transport limited by conduction at tube-to-tube junctions, can provide mobilities as high as $80\,cm^2\,V^{-1}\,s^{-1}$ (ref. [67]), which is a major advantage over polymer semiconductors. Benefiting from this, when SWCNTs are fabricated into intrinsically stretchable transistors, the resulting transistors display mobilities as high as $15\,cm^2\,V^{-1}\,s^{-1}$, accompanied by stretchability over 100%[54]. However, because the strain-induced morphological changes on SWCNT networks are usually irreversible, the strain typically has a non-negligible influence on electrical performance. In addition to such structural instability, semiconducting SWCNTs usually have inferior ambient stability[68] compared with polymer semiconductors.

Intrinsically stretchable dielectrics. In contrast to the inherent lack of stretchability of semiconductors, stretchable dielectrics have been readily accessible since the first discovery of rubber. Several existing elastomers, including polydimethylsiloxane (PDMS) and polystyrene-block-poly(ethylene-ran-butylene)-block-polystyrene (SEBS), have been utilized as gate dielectrics to achieve intrinsically stretchable transistors with good operation stability[59,62]. However, the main limitation of these non-polar elastomers is their relatively low dielectric constants (in the range of 2–3), which lead to a high operation voltage (>10 V) for the resulting stretchable transistors. To overcome this limitation, research efforts have been devoted to finding or creating elastomers with higher dielectric constants, either by exploring more polar elastomers, such as poly(vinylidene fluoride-co-hexafluoropropylene) (PVDF-HFP) and polyurethane (PU)[69], or compositing with non-stretchable high-κ fillers[70]. However, these high-κ elastomers tend to facilitate the delocalization of ionic impurities, often leading to an electrical-double-layer effect and thus a frequency-dependent performance[71]. On the other hand, such an electrical-double-layer effect can be utilized to largely decrease the operation voltage when the transistors are not used for high-frequency applications. This is exemplified by the use of ionic gels (made with intrinsic stretchability) as stretchable dielectrics[72,73], which give an operation voltage lower than 2 V and an operation frequency up to 1 kHz.

Besides the intrinsic material property, the film quality of the as-fabricated dielectric layers is the other equally important factor for achieving higher capacitance and thus lower operation voltage. Therefore, innovations in conformable film deposition methods for such elastomeric films are also greatly needed.

Scalable fabrication of intrinsically stretchable transistors. With the availability of intrinsically stretchable materials, the next main challenge in the development of intrinsically stretchable electronics is the scalable and reliable fabrication of integrated transistors and circuits[74,75]. Because of the differences in many physicochemical properties of inorganic materials, most polymers are incompatible with lithography-based microfabrication processes. This has been a long-standing challenge for polymer electronics over the past 40 years, since its inception. Recently, our research has successfully filled this gap through the development of a fabrication platform for intrinsically stretchable transistor arrays (Fig. 5c(i))[74]. The key innovations in this fabrication platform include a direct photo-patterning process for dielectrics (Fig. 5c(ii)), an etching-based patterning process for polymer semiconductors and effective harnessing of orthogonal polymers as sacrificial layers. This platform has been shown to have broad material applicability, without any sacrifice in performance. Furthermore, the achieved transistor arrays have demonstrated the expected advantages of intrinsically stretchable electronics: scalable fabrication with a high yield of 94% and a high density of $347\,cm^{-2}$ (Fig. 5c(iii)).

Perspective. In pursuit of stretchable ICs with complex functions for practical applications, there are still several major aspects to be improved: increasing the mobility, which needs innovations in molecular design and processing methods for polymer semiconductors; reducing the operating voltage from the current level of 30 V to below 5 V, which needs the development of stretchable dielectrics with higher permittivity in conjunction with the invention of conformable film deposition methods; miniaturization of devices and increasing the device density, which needs further innovations in fabrication methods together with a significant improvement in charge injection at the electrode contacts[76,77] to alleviate the short-channel effect; and developing n-type stretchable transistors. Other challenges faced by polymer semiconductors also need to be taken into consideration during the developmental efforts, including insufficient ambient stability, imperfect thin film uniformity and batch-to-batch variations in polymer synthesis. The first demands the identification and/or development of a stretchable encapsulation material with good air impermeability. The latter two could be improved by the development of precision synthesis methods and improvements in thin-film deposition processes for polymer semiconductors.

Applications of stretchable transistors and circuits

In general, transistors in electronic systems are mainly used for signal processing between input and output terminals, and can be categorized into three general functions: multiplexing, analogue signal conditioning and digital computation. Transistors are also utilized as sensing elements for various types of signal. Proof-of-concept demonstrations have shown that stretchable transistors can perform all four functions (Fig. 6a), suggesting future work on developing fully functionalized stretchable systems.

Sensing. When serving as the transduction device for sensing, transistors can typically offer higher sensitivity than other device options, afforded by their built-in signal amplification function. A large group of sensing mechanisms and material/device designs have been developed by using transistors for sensing different types of signal[78,79]. An early work demonstrated an intrinsically stretchable temperature sensor based on a transistor-like structure that employs a temperature-sensitive and stretchable composite as the channel material[80]. More recently, fully CNT-based stretchable transistors were developed for temperature sensing by taking advantage of the temperature-dependent behaviour of charge transport in semiconducting SWCNT networks (Fig. 6b)[81]. The most important advancement in this work is the use of a differential circuit design strategy to suppress the influence of strain on the readout signal. Moving forward, there are many more innovations to be explored towards realizing sensing functions for different types of signal (pressure, vibration, moisture and various biomarkers) based on different material/device designs. Regardless of the application, to achieve reliable sensing performance under

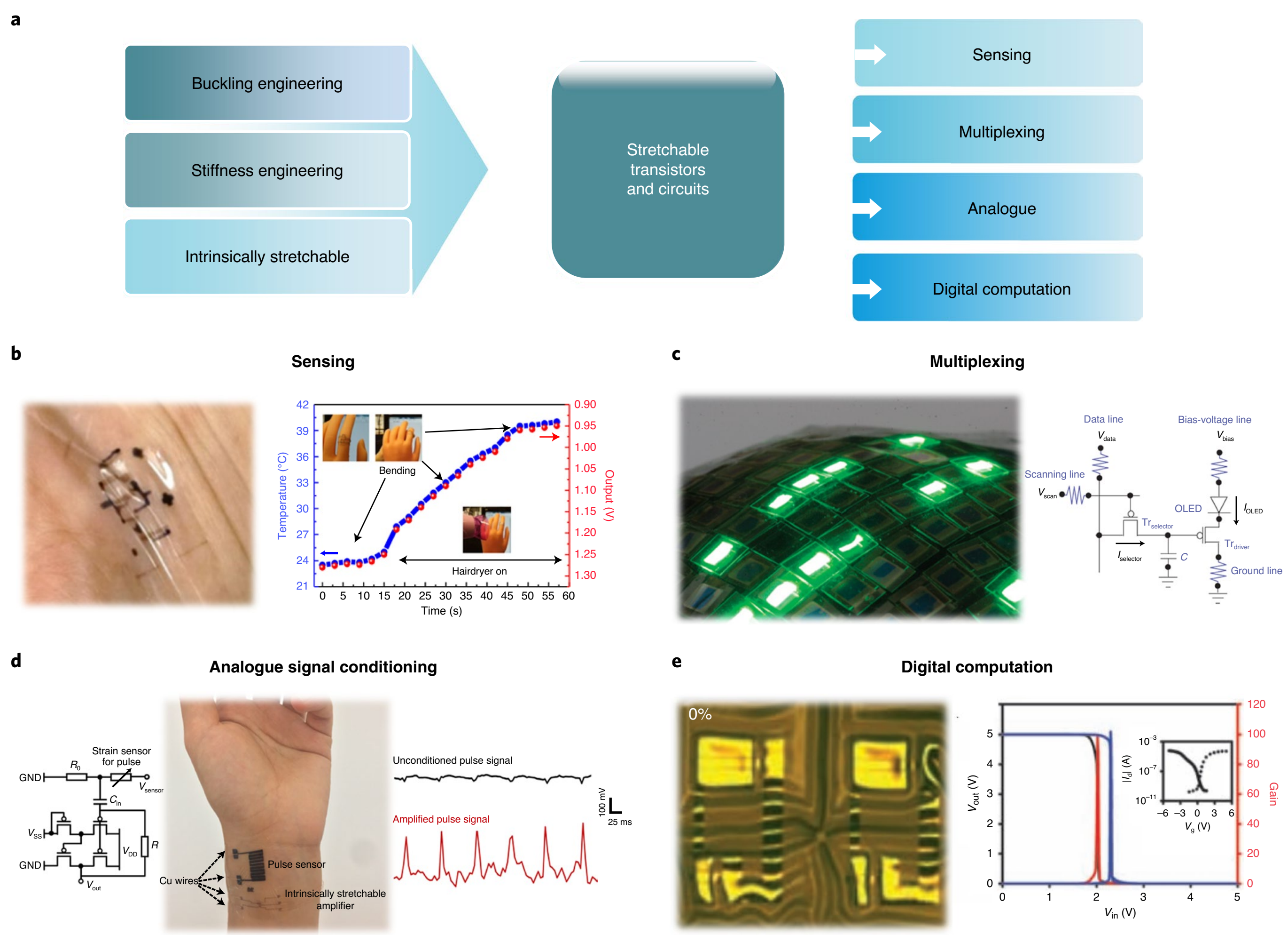

Fig. 6 | Applications for stretchable transistors and circuits. **a**, Summary of main application areas. **b**–**e**, Representative examples for the different application areas: stretchable temperature sensor (**b**); stretchable active-matrix organic light-emitting diode (AMOLED) array (**c**); stretchable sensor–amplifier system for pulse measurements (**d**); stretchable digital circuits (inverter) (**e**). Figure reproduced with permission from: **b**, ref. [81], Springer Nature Ltd; **c**, ref. [40], Springer Nature Ltd; **d**, ref. [74], Springer Nature Ltd; **e**, ref. [22], AAAS.

stretching, sensor designs need to decouple the influence of strain from the sensing functions.

Multiplexing. For signal reading and writing from/to arrayed input/output (I/O) devices such as sensors and light-emitting diodes, multiplexing operation is generally favoured to avoid crosstalk and to reduce the number of wirings. Multiplexing has been realized by an array of transistors, namely an 'active matrix', in which each transistor or small group of transistors addresses one I/O device element. So far, this has been realized in a number of stretchable electronic systems. For example, using stiffness engineering designs, rigid silicon[82,83] and organic small-molecule transistors[40] have been integrated with their corresponding functional devices (for example, light-emitting diodes) on rigid islands, which are supported by an elastomer substrate to enable global stretchability (Fig. 6c). Additionally, recent work has demonstrated the fabrication of an intrinsically stretchable active matrix interfaced with a tactile sensor array, with the advantages of high device density (25 pixels cm^{-2}) and outstanding skin conformability[74]. Overall, given that the aim of arrayed integration is usually to achieve high density, the intrinsically stretchable approach could be more favourable for building an active matrix. To move forward in realizing higher working frequencies and further reduced crosstalk, it is necessary to upgrade the 1-transistor (1T) design that is currently prevalent in demonstrated stretchable arrays to more complicated structures such as 2-transistor–1-capacitor (2T1C) designs[84].

Analogue signal conditioning. Biological and physiological signals are among the chief measurement targets for stretchable electronics. However, they are typically weak in amplitude/intensity and are therefore easily affected by interference from various types of background noise. Hence, robust amplification and filtering are needed for the effective recording and processing of such signals. In early research into buckling engineering of silicon transistors, differential amplifiers with a stretchability of 5% strain were demonstrated[22]. Intrinsically stretchable transistors, which exhibit superior conformability with the skin, could be a preferred choice for providing on-site amplification by directly interfacing with skin and tissue. Recently, a first generation of an intrinsically stretchable transistor array was realized using self-biasing pseudo-CMOS designs, achieving a gain of 4.7, a frequency bandwidth of ~50 Hz and a stretchability of over 100% strain (Fig. 6d)[74]. In future work towards achieving effective amplification of different types of bio-signal, material and device innovations are needed to maximize the gain and bandwidth. Also, based on the achieved amplifiers, stretchable filters and analogue-to-digital converter (ADC) circuits are waiting to be realized, which can be designed with relaxed requirements for skin conformability.

Digital computations. In most advanced electronic systems, the 'brains' are typically processors (central processor units and microprocessors) that implement algorithms with different functions. Such processors usually contain millions of transistors, with logic gates as the building-block elements. So far, several types of logic gate have been realized, including inverters (Fig. 6e)[22], NAND and NOR gates, and ring oscillators, with stretchability ranging from 5% to 100% strain[74,75,85]. The potential functions of logic gates in stretchable systems generally include wireless communications, d.c.-to-a.c. signal conversions and further integration into processors. Among these, the integration of stretchable logic gates into processor development is the most challenging due to the need for an exceptionally large number of devices. This poses very demanding requirements in terms of device yield, performance uniformity and device density. As the processor module is the central information processing hub, it does not necessarily need to be placed at the skin/tissue location for signal collection and/or delivery. It could therefore be located in body areas where relatively lower strains are created. As such, the stiffness engineering approach for the incorporation of commercial silicon chips could be a highly viable option for introducing digital computations into stretchable electronic systems.

Outlook

Three technological pathways have been established for creating stretchable transistors and circuits — buckling engineering, stiffness engineering and intrinsic-stretchability engineering — and proof-of-concept applications have been demonstrated. However, challenges remain in terms of material innovation, device fabrication and circuit design architecture. In addition, to maximize the utility of the technology, a broad understanding is required of the pros and cons of these general approaches in terms of their different functionalities and applications.

The design of stretchable transistors is still based on the device physics of silicon transistors. However, the involvement of substantial mechanical strain during device operation and the use of unconventional device structures give rise to relatively unexplored device physics. A deeper understanding of the device physics of stretchable transistors will provide important information for the design and optimization of such transistors along all three engineering pathways. Furthermore, improvements in both electronic performance and mechanical robustness will largely come from the continuous development of stretchable functional materials, including conductors, semiconductors and insulators. For semiconductors and conductors, excellent charge-transport capabilities — characterized by mobility and conductivity — are needed. Additionally, precise control of electronic structure and charge-carrier density are required to build high-performance devices. Developments in stretchable insulators are also needed to improve substrates, dielectrics and stable packaging layers with minimal oxygen and water permeability.

At the device level, substantial enhancements in device densities are needed to build complex circuit structures within reasonable device areas. Such improvements will come from the creation of new fabrication methods and optimization of the fabrication of multiscale mechanical structures. Furthermore, the strategy of stacking 2D device layouts into multilayer 3D architectures could deliver a substantial increase in device densities. Developments in the large-area fabrication of stretchable transistors will also be important, preferably using additive manufacturing processes, which can better take advantage of solution-processable materials with low-cost production. The larger device counts required for more complex circuit designs will, however, create much higher requirements in terms of device yield and uniformity, creating another key challenge that will need to be resolved.

Finally, the application of complicated circuits also demands a materials-to-device strategy for effective thermal control, because the low thermal conductivities of elastomers necessitate the addition of heat-dissipation designs. Systematic progress in the creation of circuits with higher complexities will require the development of compact models for transistor structures operating under stretching, the realization of CMOS units and circuit design strategies for mitigating strain effects.

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Y.D., H.H. and S.W. researched the data and wrote the manuscript. M.W. and J.X. reviewed and edited the manuscript. All authors discussed the contents and provided important contributions to the manuscript.

Competing interests
The authors declare no competing interests.

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